

ATLAS upgrades for the HL-LHC

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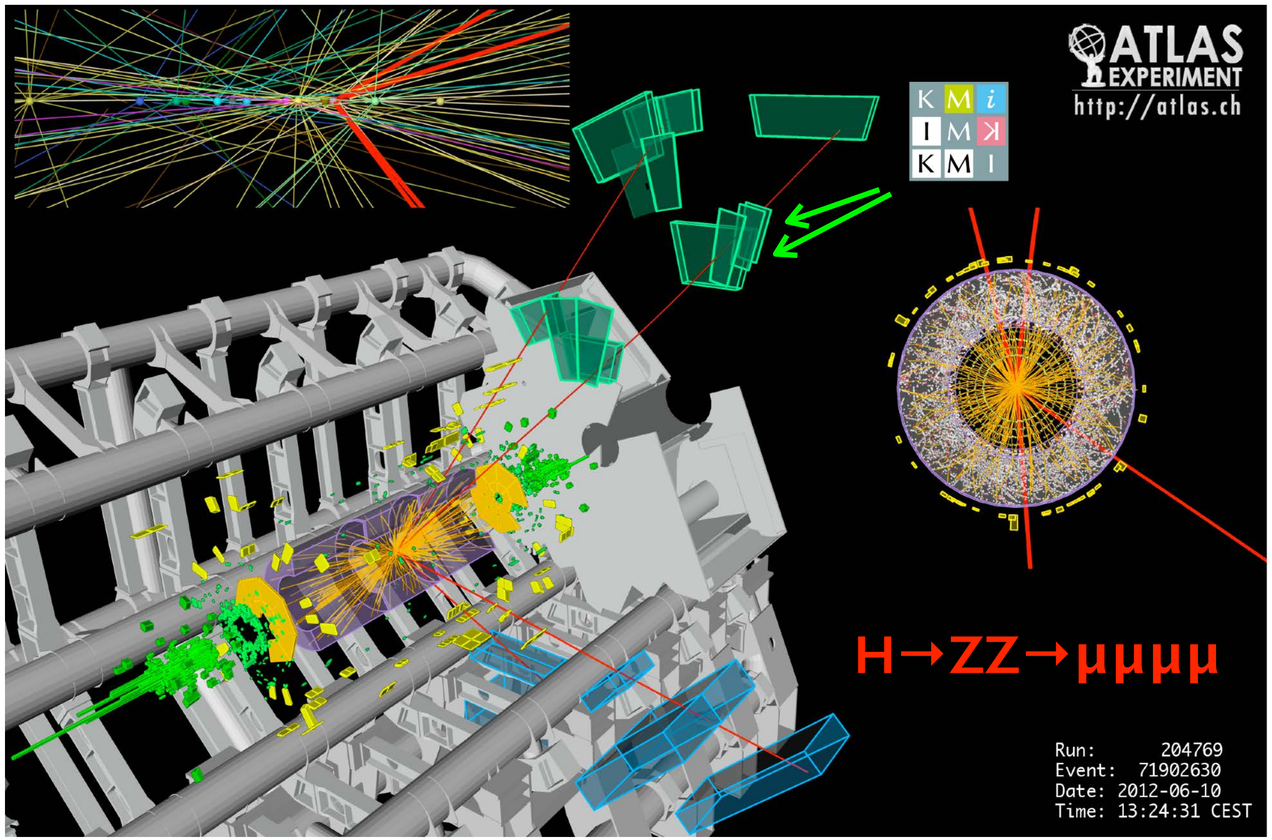
KMI 2026, 9 Nov. 2023

Higgs Boson Observation in 2012

The Higgs boson observed in 2012

F. Englert and P. W. Higgs awarded the Nobel Prize in Physics in 2013



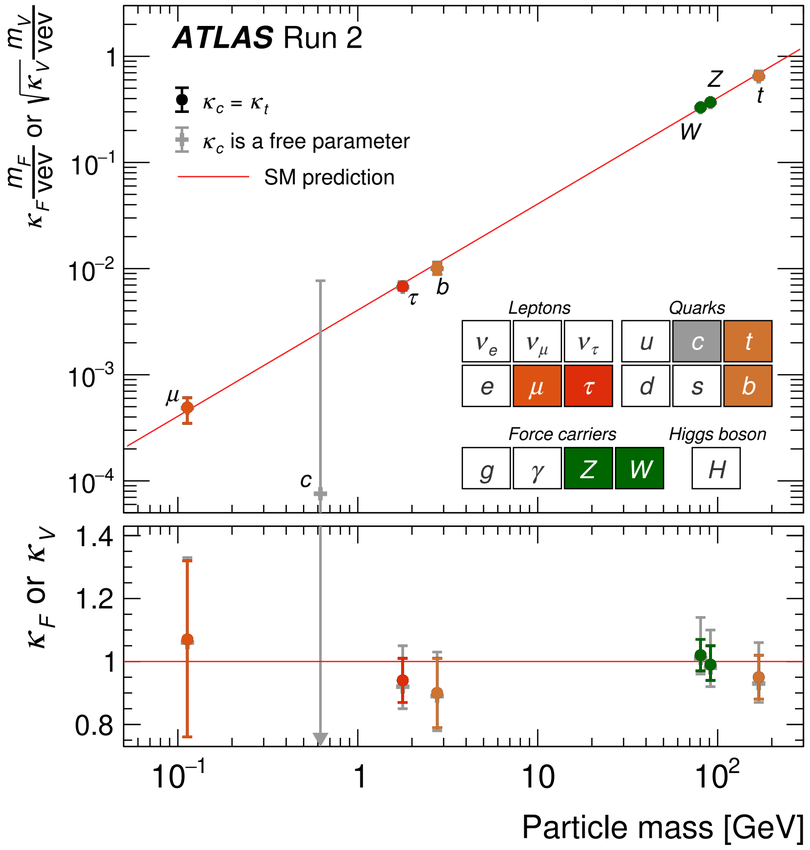




Probing the Origin of Particle Masses

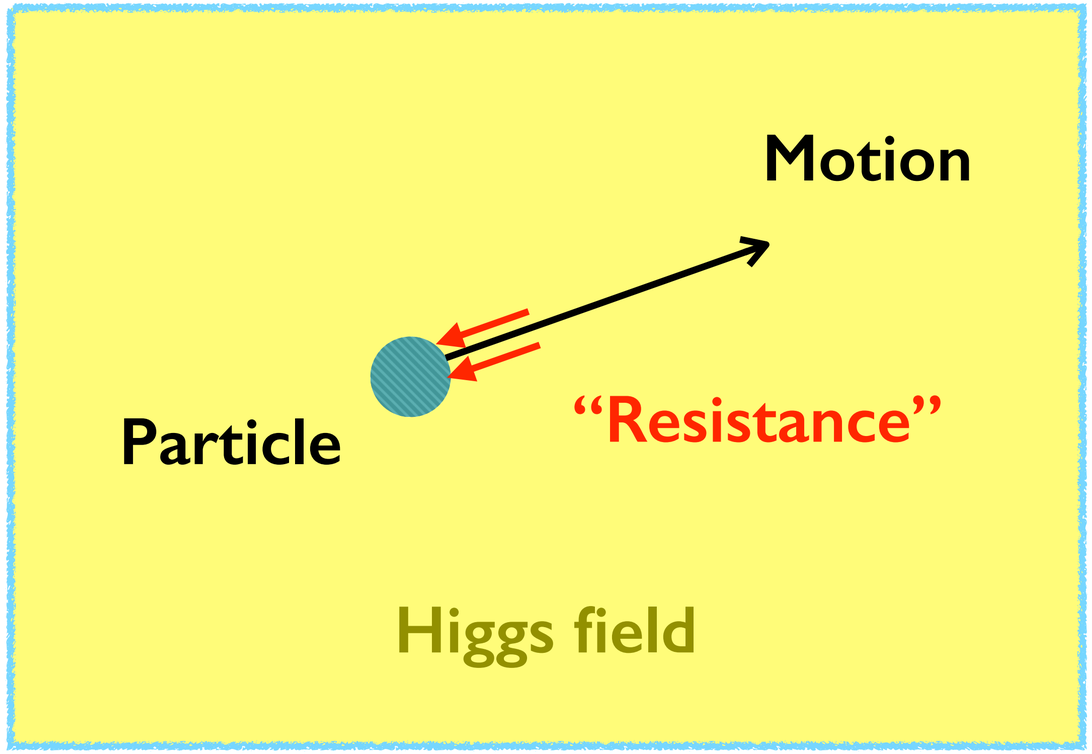
Higgs boson coupling measurements are consistent with the Standard Model, supporting the Higgs mechanism as the origin of masses of Z, W, t, b, and τ.

Nature, 2022



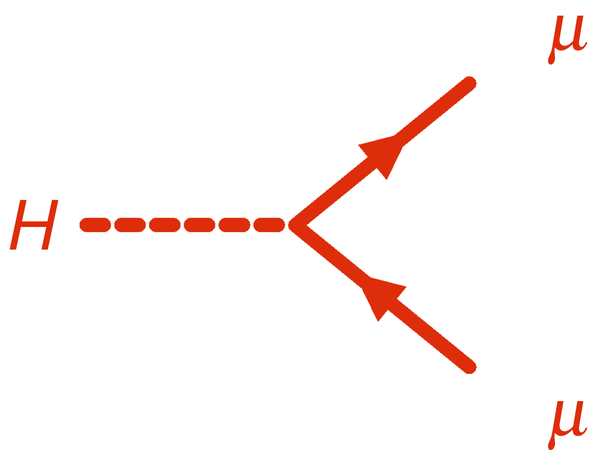


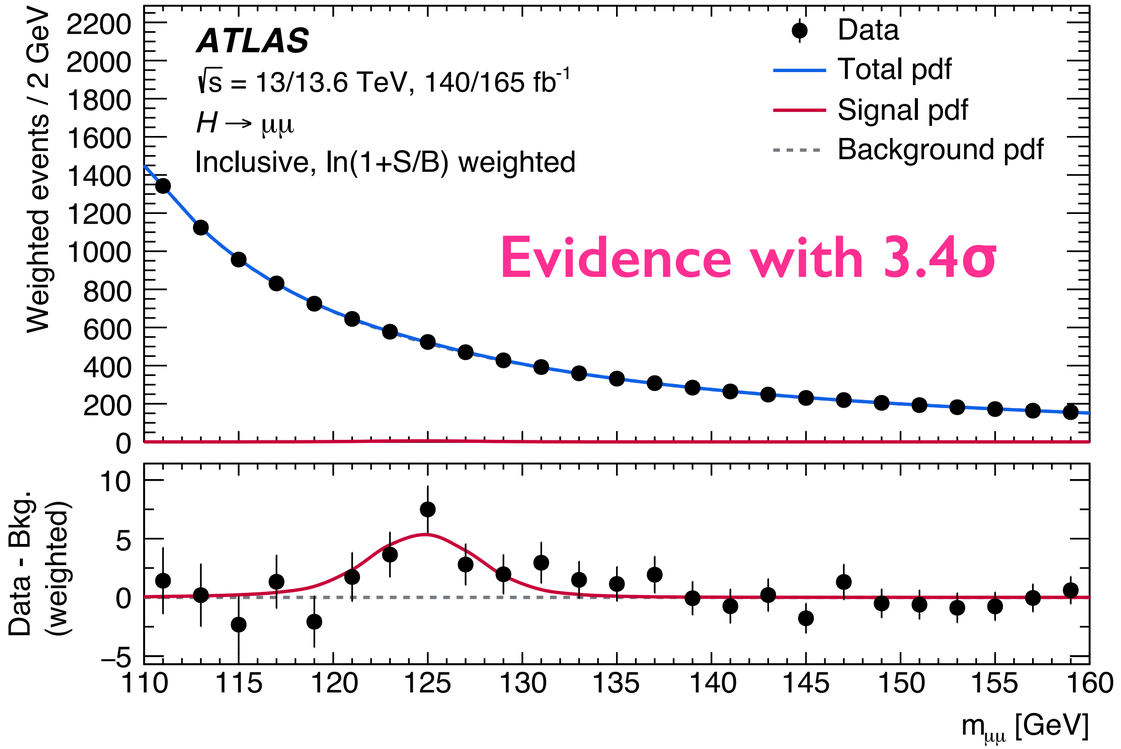
Doctor's degree:
T. Kawaguchi
for H→μμ (2021)
Y. Mitsumori
for H→ττ (2025)



A New Result for H→μμ

Probe of the Higgs coupling to muon





Signal strength relative to the Standard Model prediction: 1.4 ± 0.4

— evidence for the origin of muon mass through the Higgs field

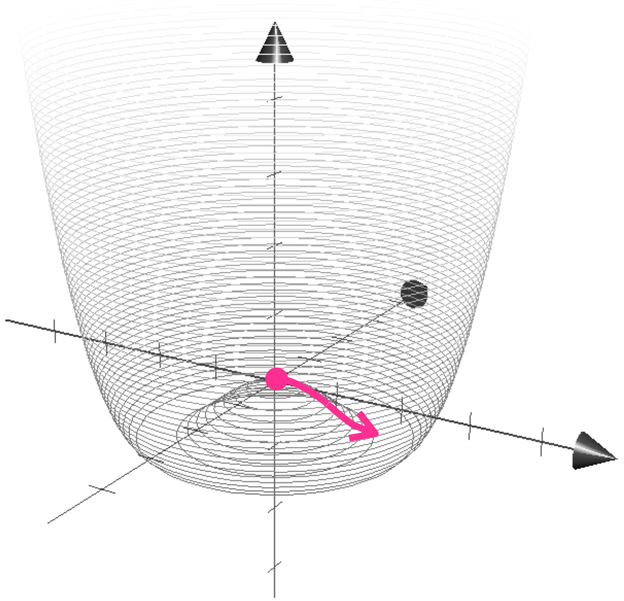
PRL 135, 231802 (2025)

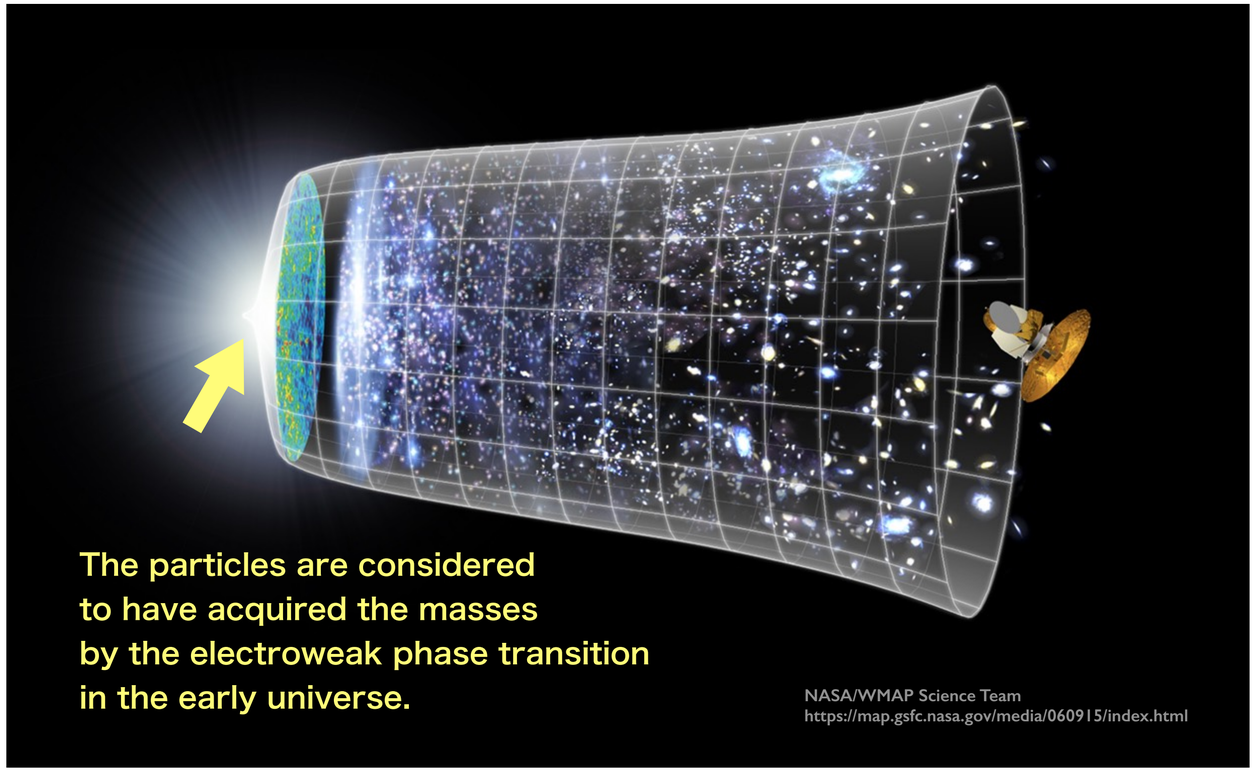
Candidate of doctor's degree: A. Wada

A Next Step: Exploring the Higgs Potential

May probe the electroweak phase transition and vacuum stability

Higgs potential $V(\phi)$

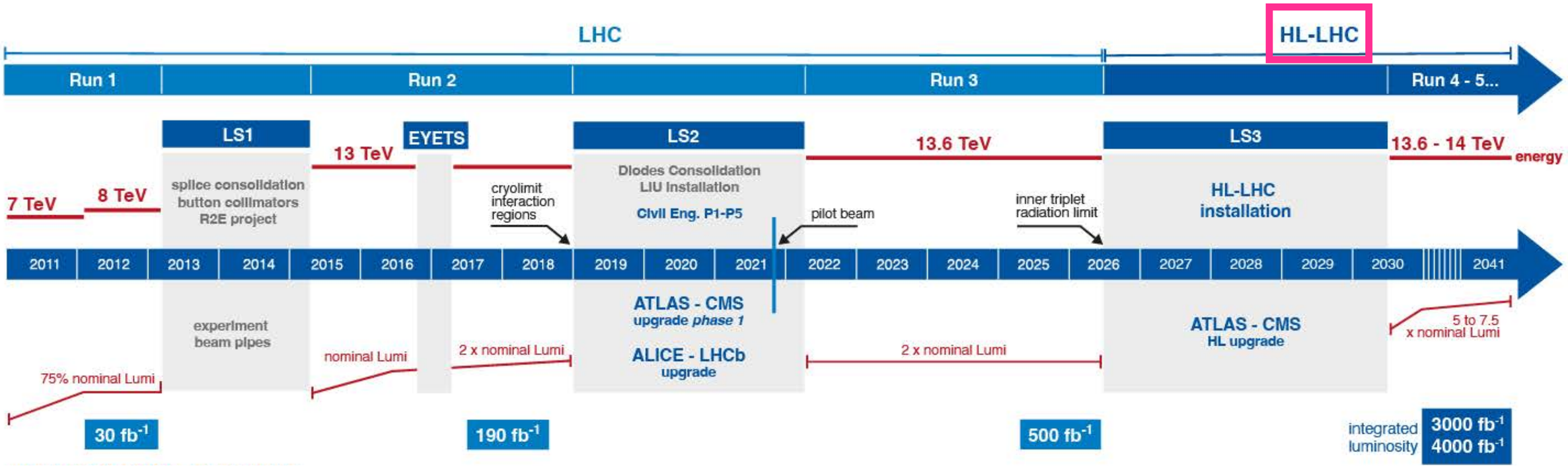




Search for Higgs boson pair production with 4b: PRD 108, 052003 (2023) — Doctor's degree: S. Hayashida (2023)

Top quark mass measurement using J/ψ→μμ: JHEP 04 (2026) 099 — Doctor's degree: H. Asada (2026)

LHC Upgrade toward HL-LHC



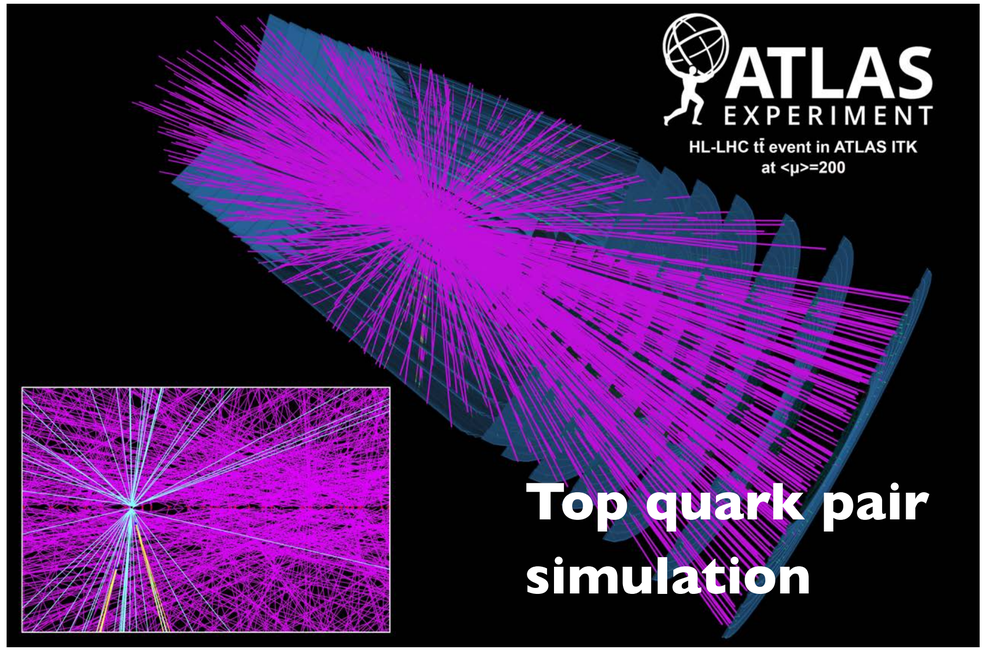
Luminosity upgrade: 2 x 10^{34} $cm^{-2}s^{-1}$ → 5–7.5 x 10^{34} $cm^{-2}s^{-1}$

Start of the operation in 2030

Challenges for HL-LHC

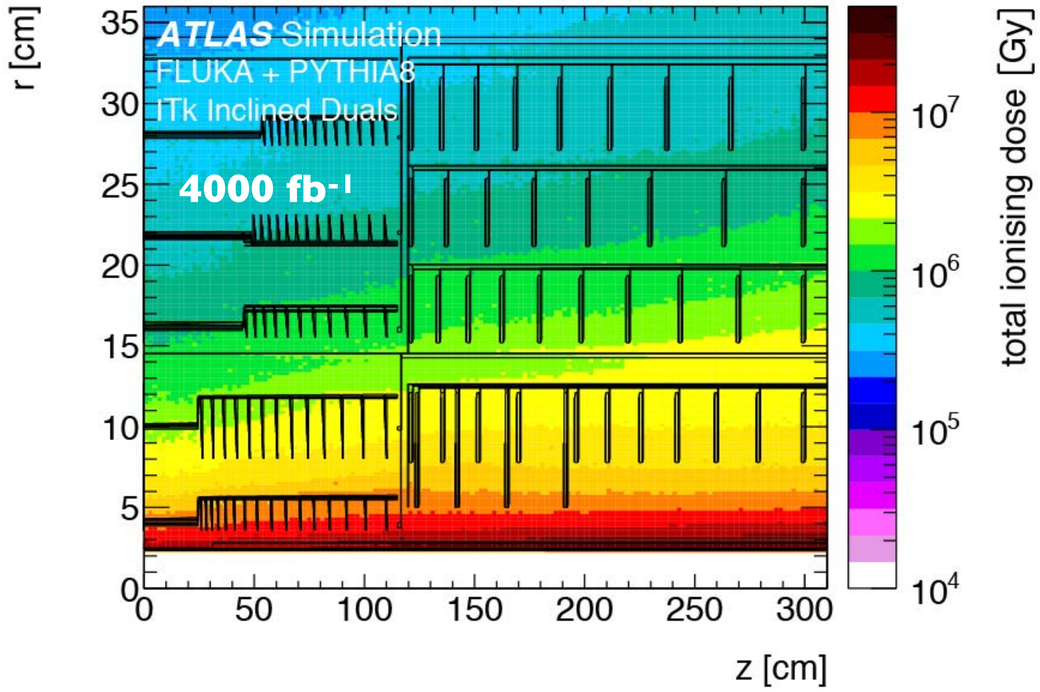
High luminosity, high pileup (high number of proton-proton collisions per proton-bunch crossing), high radiation level

Pileup 200

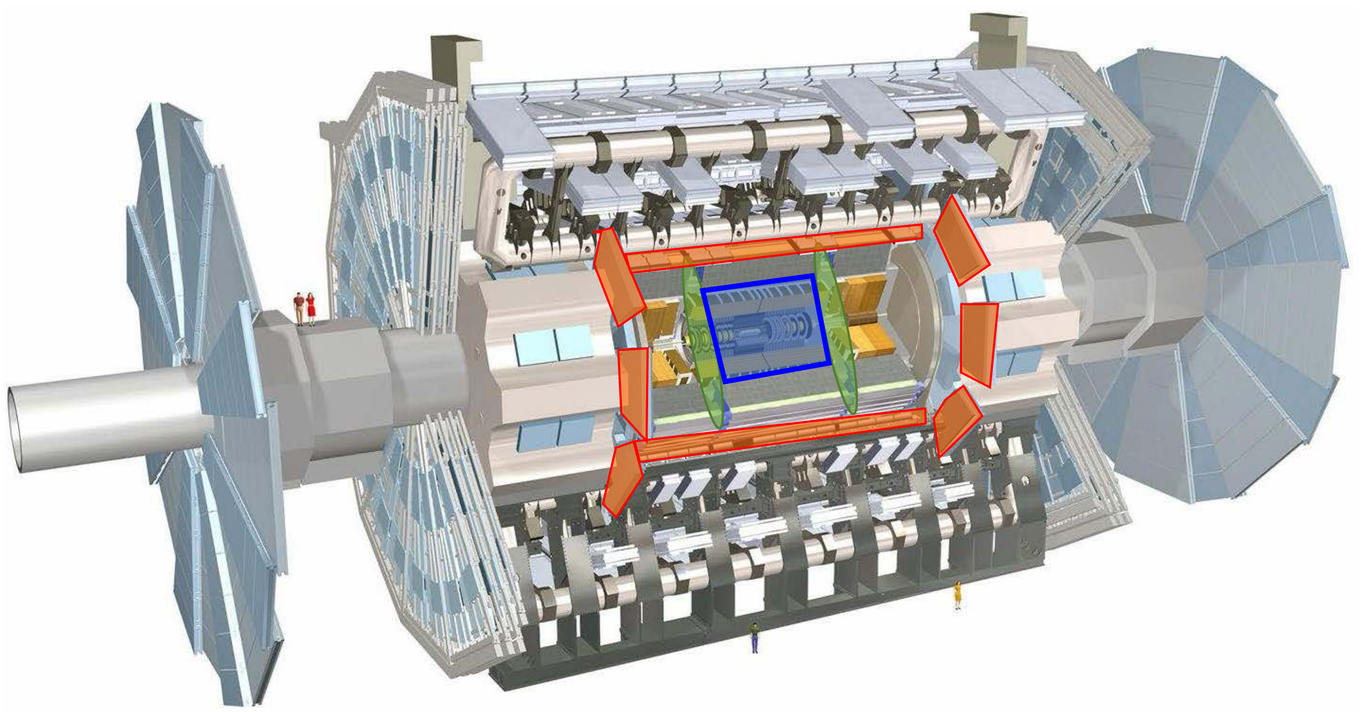


Total Ionising Dose: maximum 20 MGy

1 MeV neutron Eq. flux: maximum 2.6 x 10^{16} cm^{-2}



ATLAS Upgrades for HL-LHC



New Inner Tracking Detector
- All silicon with at least 9 layers for each track
- Less material, finer segmentation

New Muon Chambers
- Inner region with RPCs, sMDTs, and TGCs
- Improved trigger efficiency and momentum resolution, reduced fake rate

High Granularity Timing Detector (HGTD)
- Precision time reconstruction (30 ps) with Low-Gain Avalanche Detectors (LGAD)
- Improved pileup separation

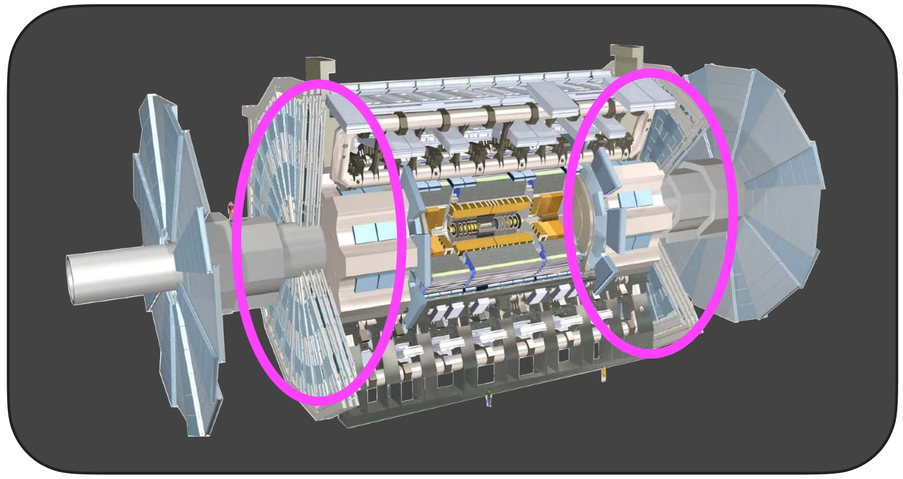
Upgraded Trigger and DAQ System
- Single level trigger at 1 MHz
- Improved 10 kHz event farm

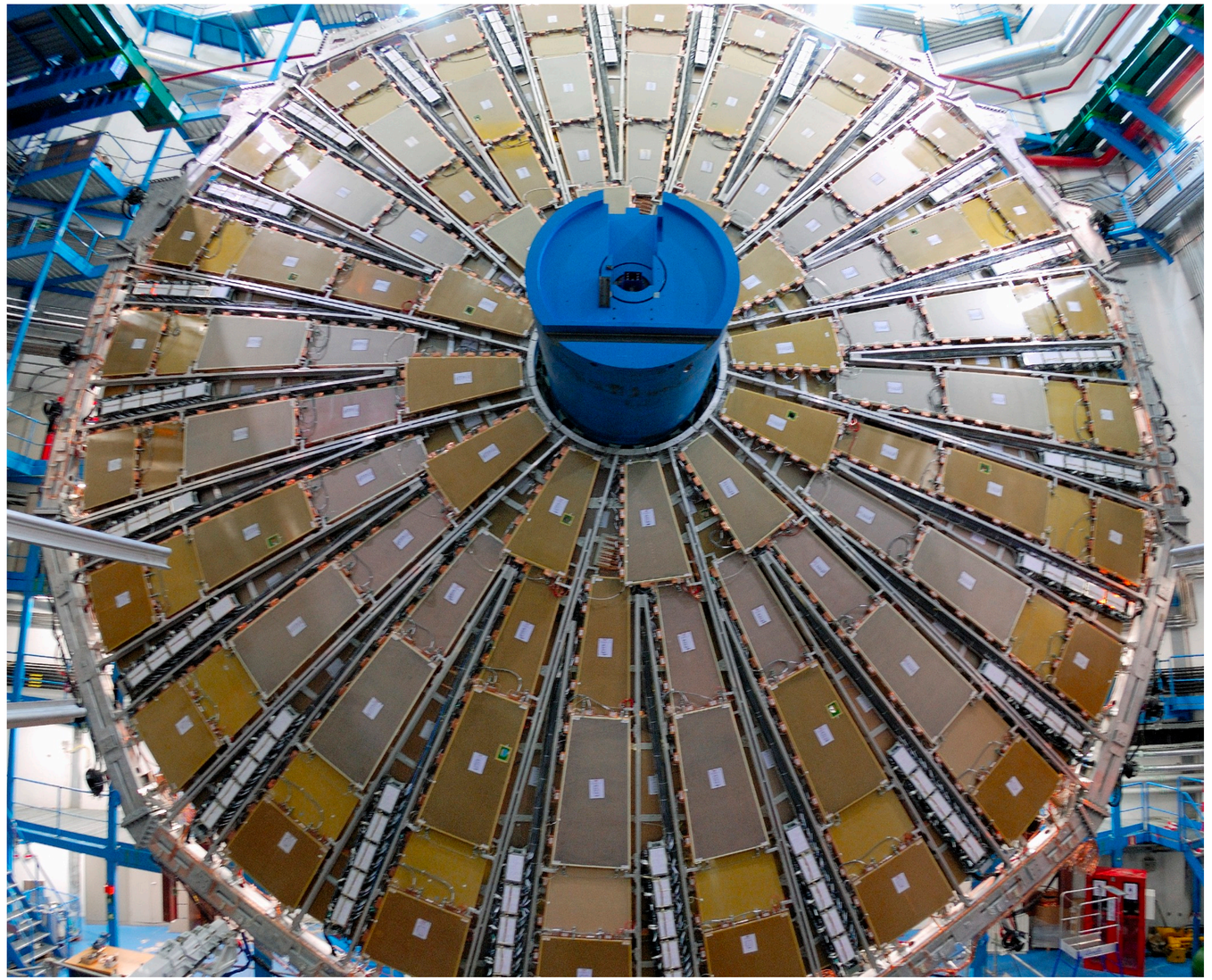
Electronics Upgrades
- On-detector/off-detector electronics upgrades of LAr Calorimeter, Tile Calorimeter, and Muon Chambers
- 40 MHz continuous readout with finer segmentation to trigger

KMI's Continuous Contributions for TGC

Thin Gap Chamber (TGC)

- Multiwire proportional chamber
- Primary role in the muon trigger
- Height: ~25 m
- Channels: ~320,000



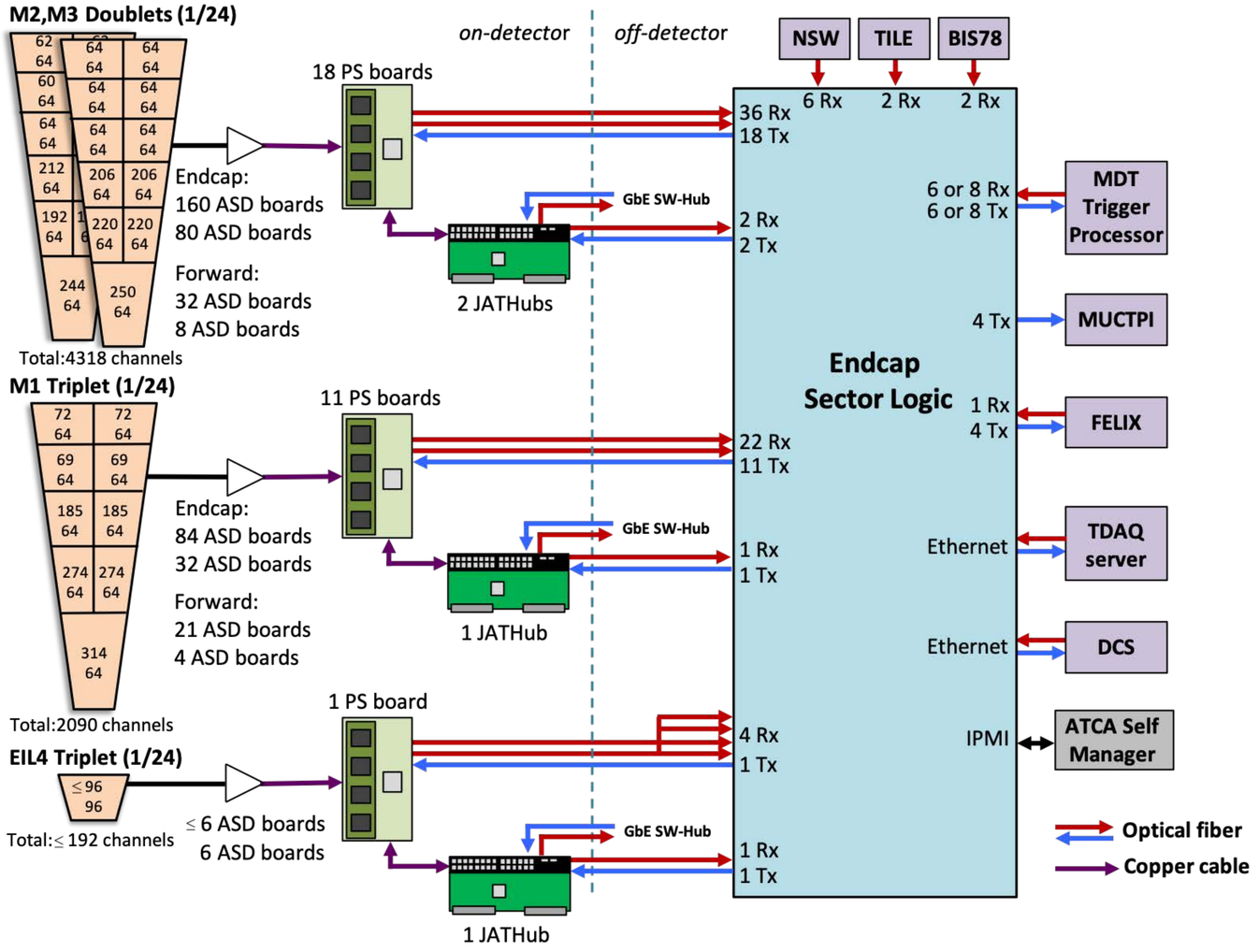


TGC Electronics for HL-LHC

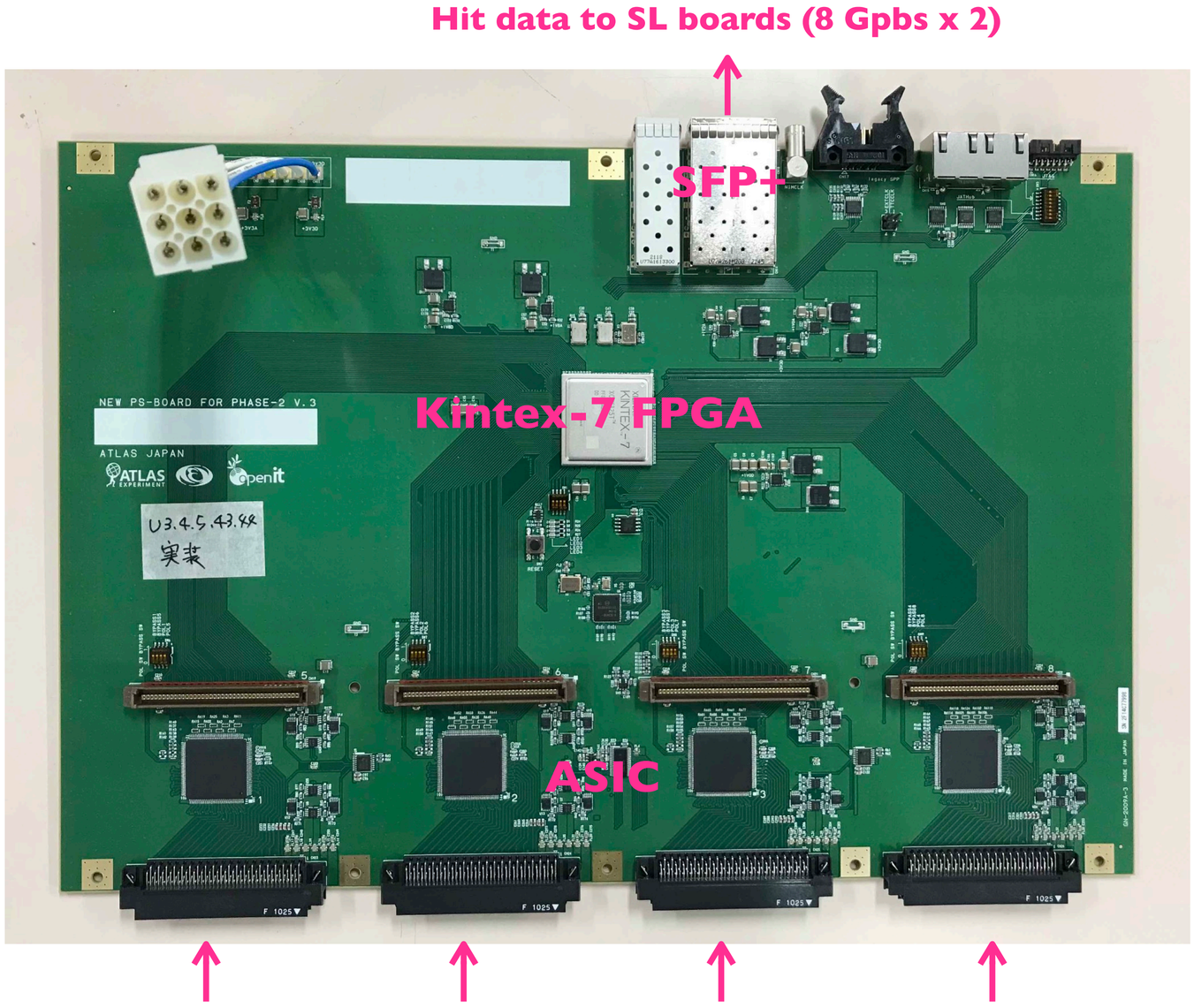
All TGC electronics boards will be replaced except for the ASD boards.

All hit data are transferred from on-detector boards (PS boards) to off-detector boards (SL boards).

Muon tracks are reconstructed in high-scale FPGAs on SL boards.



PS Board — Overview



Developments

- Schematic: master students of Nagoya
- Layout and production: company
- Tests: master students of Nagoya

Production of ~1500 boards and the quality check completed in 2025!

PS Board — Radiation Tests

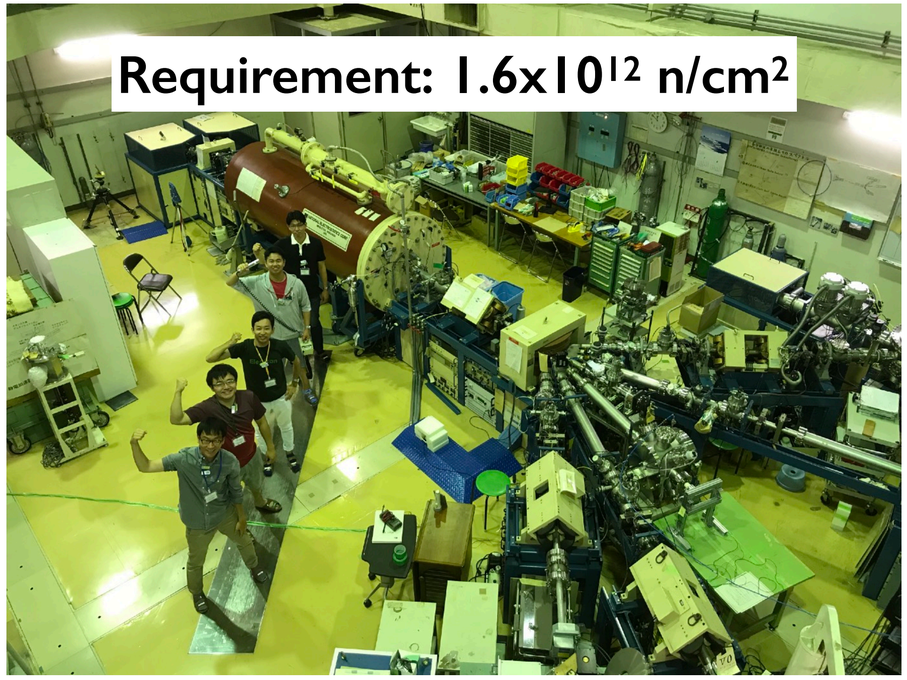
Total Ionising Dose (TID)

Gamma irradiation test
at Nagoya Univ.



Non-Ionising Energy Loss (NIEL)

Neutron irradiation test
at Kobe Univ.

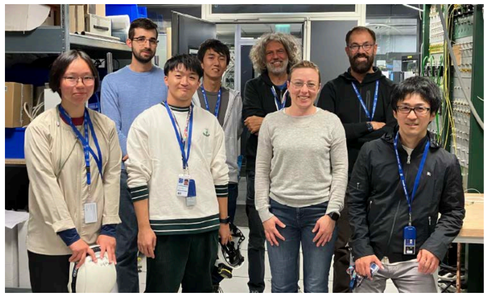


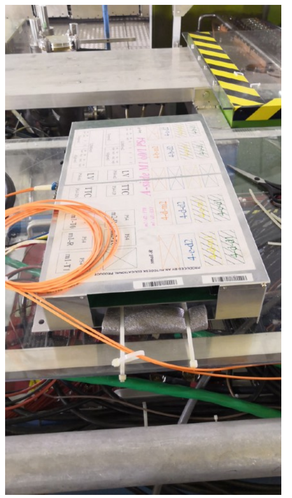
Single Event Upset (SEU)

FPGA/SFP+ SEU measurement
and recovery tests at CERN

9.8x10^2 /cm^{2}s

at L=7.5x10^{34}





Decisive role by KMI! Full radiation tests completed!

Y. Ohsumi et al., NIMA 1092, 171803 (2026)
D. Hashimoto et al., JINST 21, C04062 (2026)

PS Board — Installation

~3/4 of 1434 PS boards for the full system installed and tested!

Aim to complete the remaining ~1/4 PS boards by the end of 2026!







Leading role by KMI: employment of S. Izumiyama and dispatch of key students!

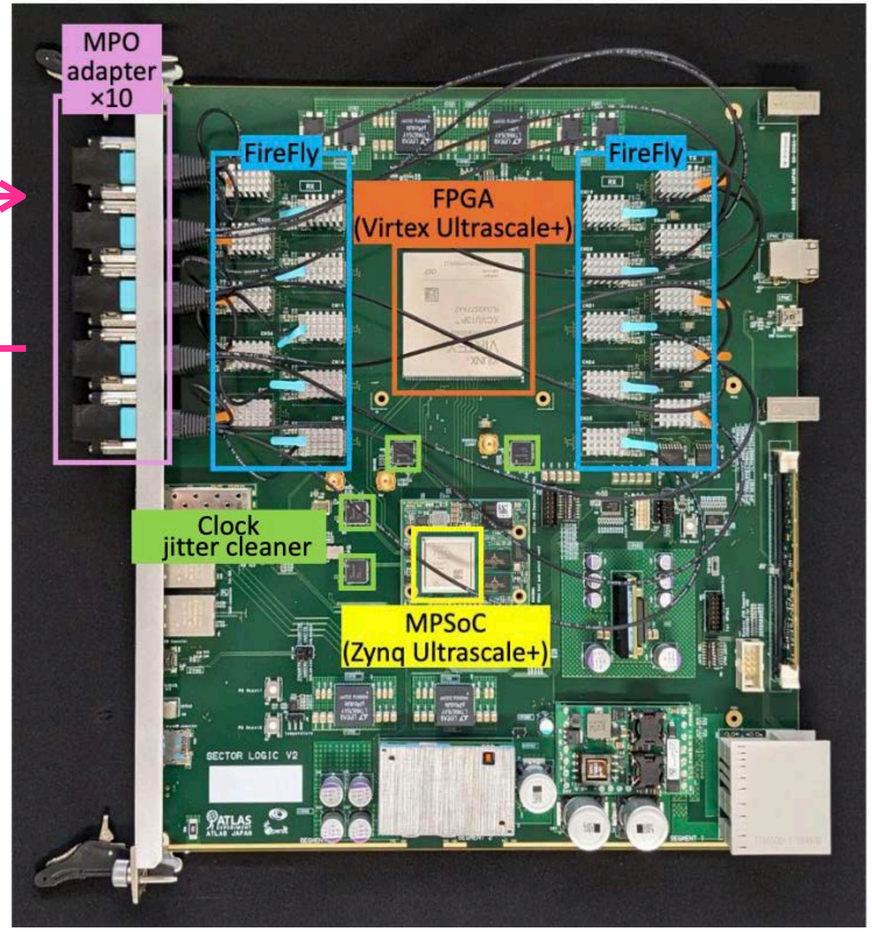
SL Board — Developments

Y. Horii: coordinator
of Level-1 muon trigger

Receives detector signals and reconstruct muons (~1 μs) for Level-1 trigger.

Detector signals →

Muon data ←



Prototyping completed

- Schematic: master students of Nagoya
- Layout and production: company
- Tests: members of the ATLAS Japan group

Algorithm studied and developed

C. Sun et al., NIMA 1045, 167546 (2023)

Making every effort to complete production and installation on schedule!

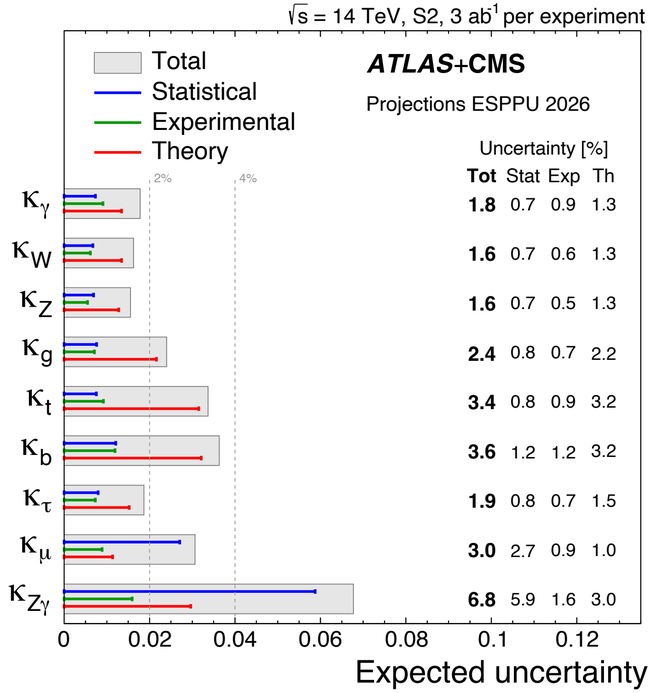
Conclusion

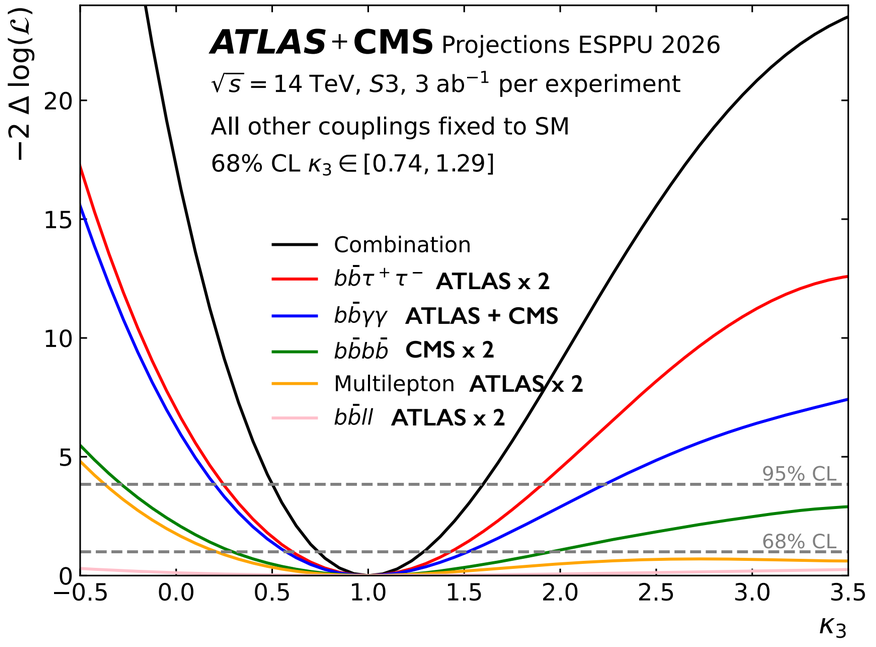
- The ATLAS experiment will be upgraded toward HL-LHC (2030-) for studies of the origin of mass, electroweak phase transition, etc.
- KMI is taking a leading role in the muon trigger upgrade.

Precise Higgs coupling measurements expected!

Higgs-muon coupling: 3.0%

Higgs self coupling: <30%

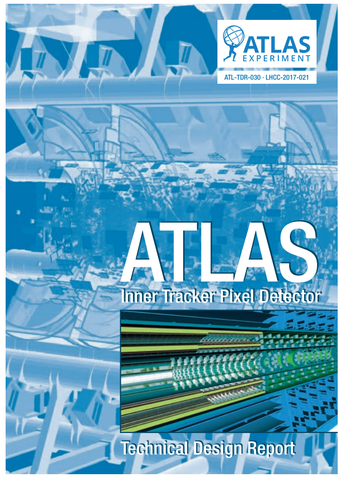




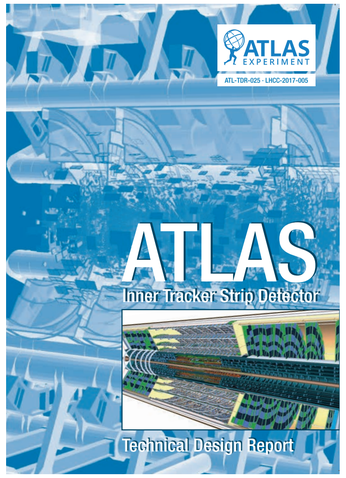
Backup Slides

Technical Design Reports (TDRs) for ATLAS Upgrades 17/15

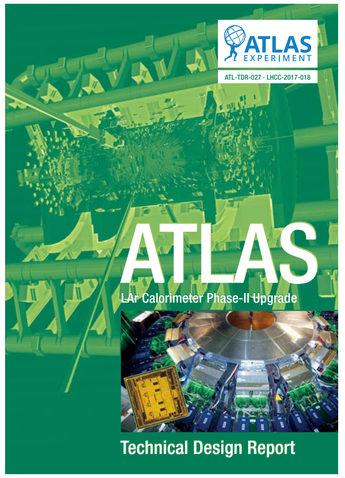
Six TDRs (~2600 pages) approved by CERN Research Board in Apr. 2018



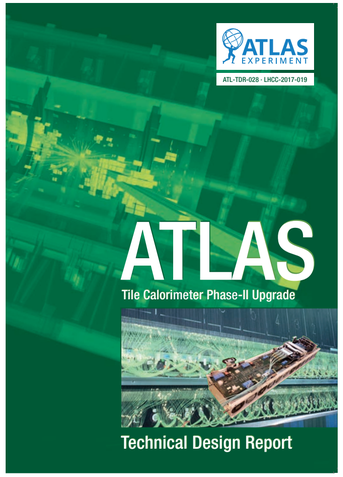
Inner Tracker
Pixel Detector
ATL-TDR-030
482 pages



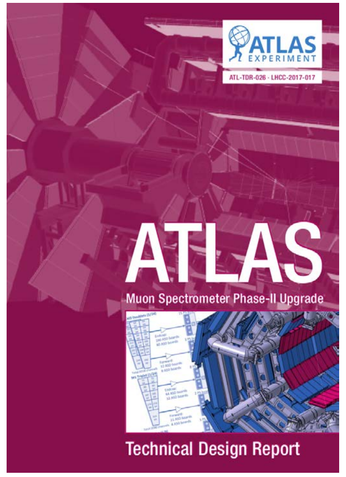
Inner Tracker
Strip Detector
ATL-TDR-025
556 pages



LAr Calorimeter
ATL-TDR-027
271 pages



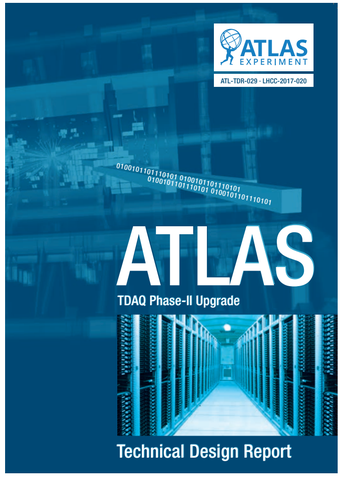
Tile
Calorimeter
ATL-TDR-028
300 pages



KMi IMK KMI

Y. Horii: editor

Muon
ATL-TDR-026
408 pages



KMi IMK KMI

Y. Horii: editor

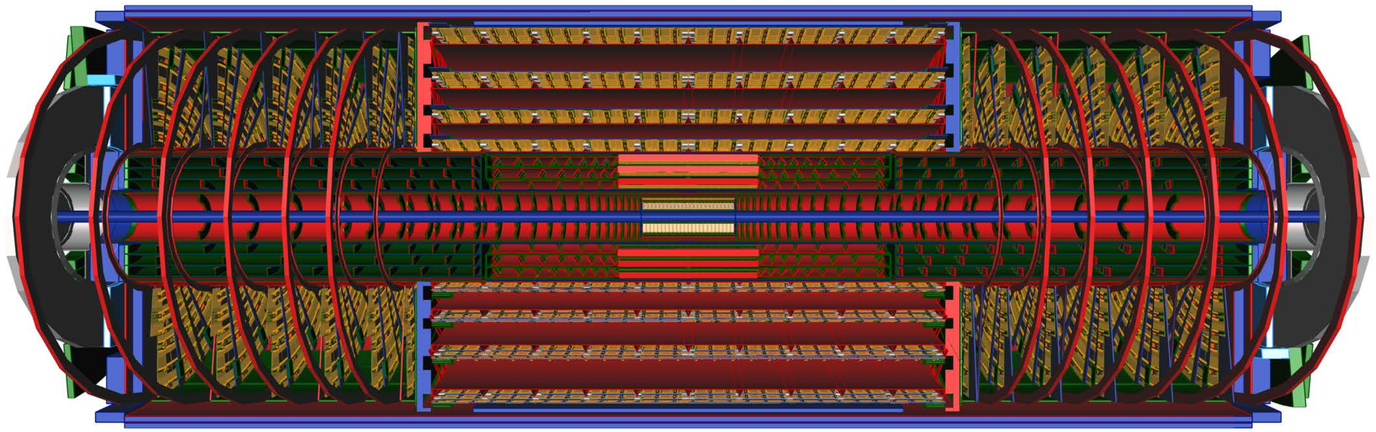
Trigger & DAQ
ATL-TDR-029
608 pages

Another TDR provided and approved later for High-Granularity Timing Detector [ATL-TDR-031]

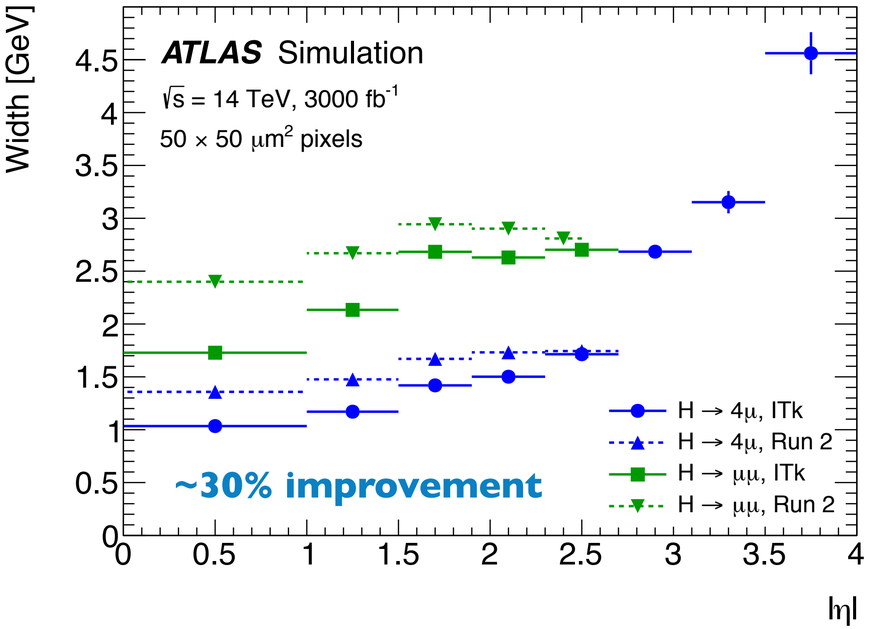
New Inner Tracking Detector

- 178 m^3 of silicon pixel + strip — factor of 2.7 larger than the current ATLAS
- Finer segmentation — improved vertexing, tracking, jet flavour tagging, …
- Coverage increased from $|\eta| < 2.5$ to $|\eta| < 4$

η: pseudorapidity



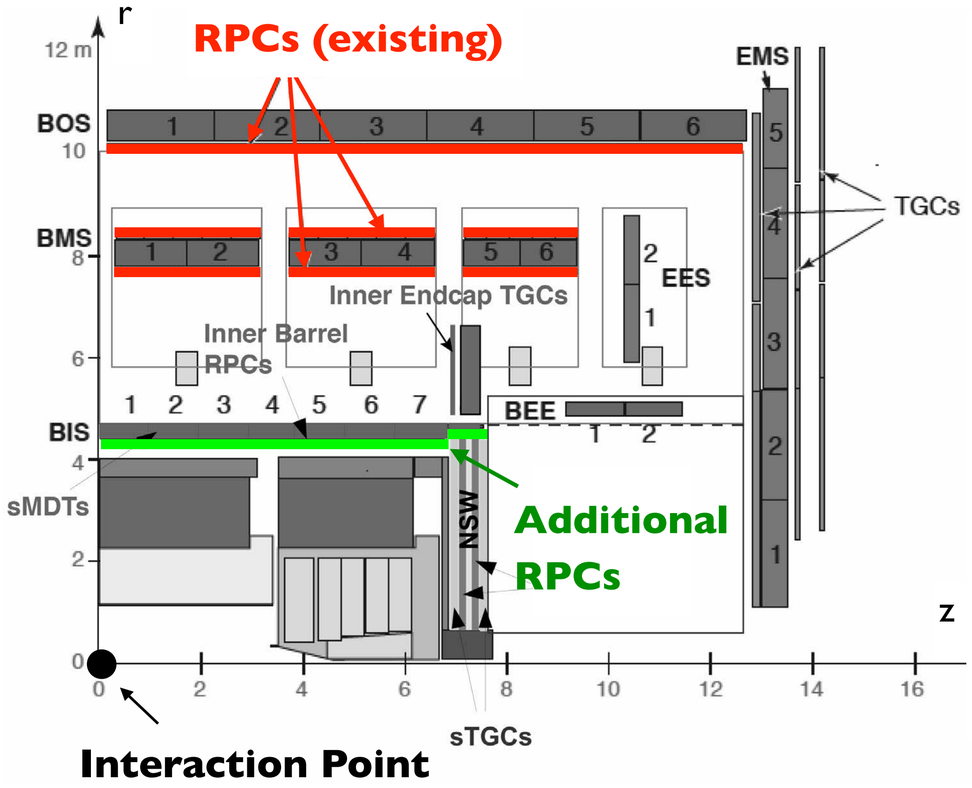
ATL-PHYS-PUB-2021-024

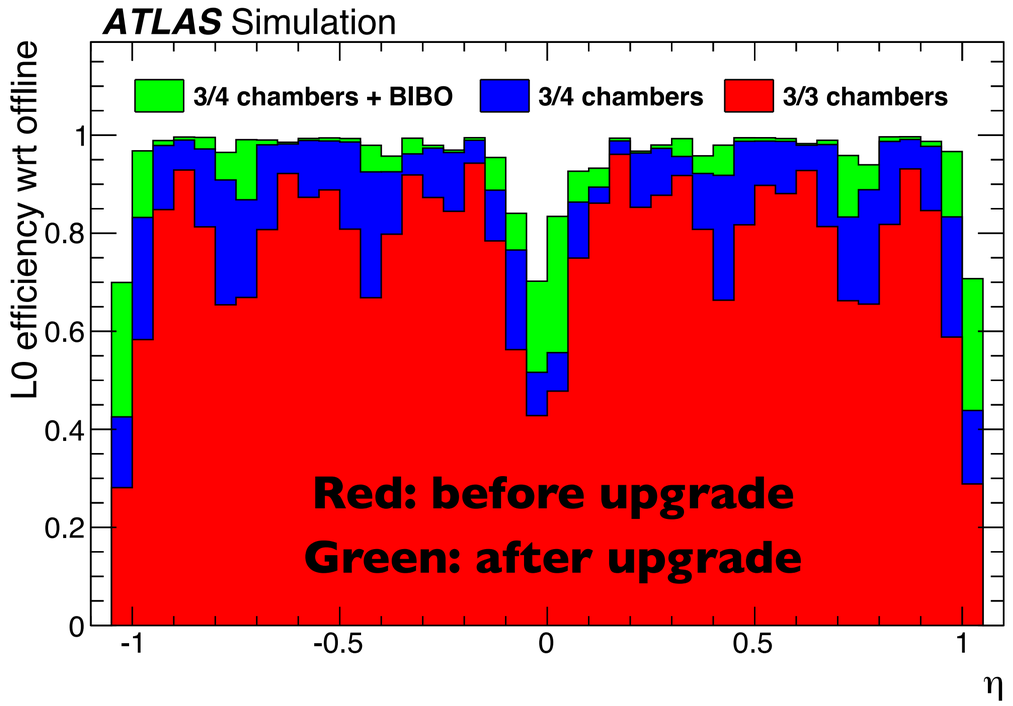


New Muon Chambers

- **Acceptance of the muon trigger in the barrel region improved by additional Resistive Plate Chambers (RPCs): 78% → 96%**

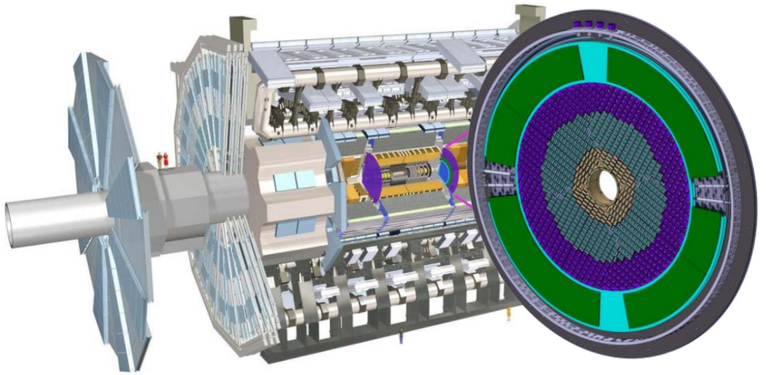
- Monitored Drift Tube (MDT) in the barrel inner layer replaced by small-diameter MDT for free space for RPCs.
- Doublet Thin Gap Chambers (TGCs) in the endcap inner layer replaced by triplet TGCs for fake reduction.

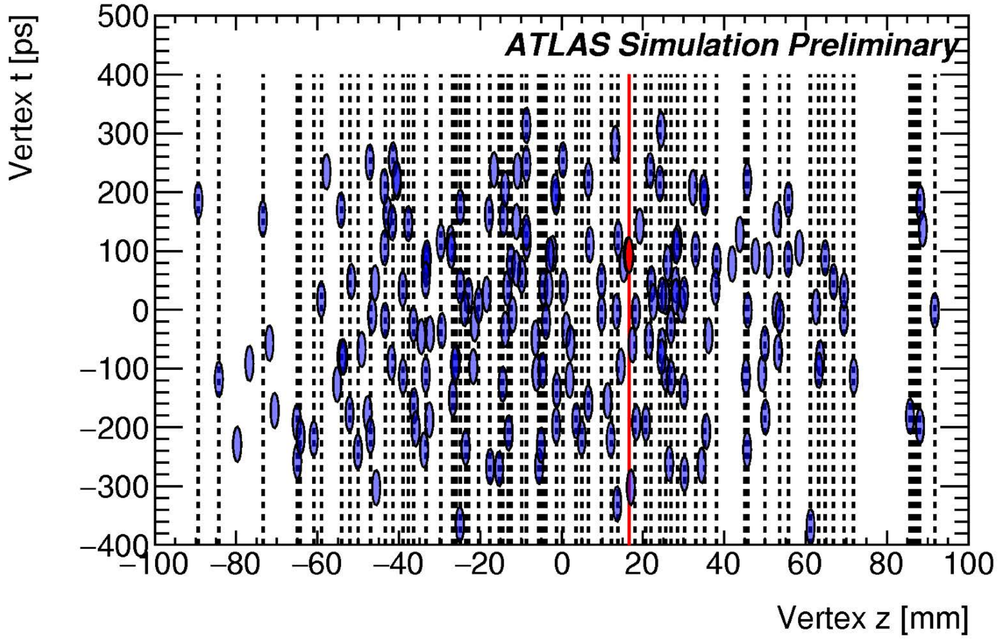


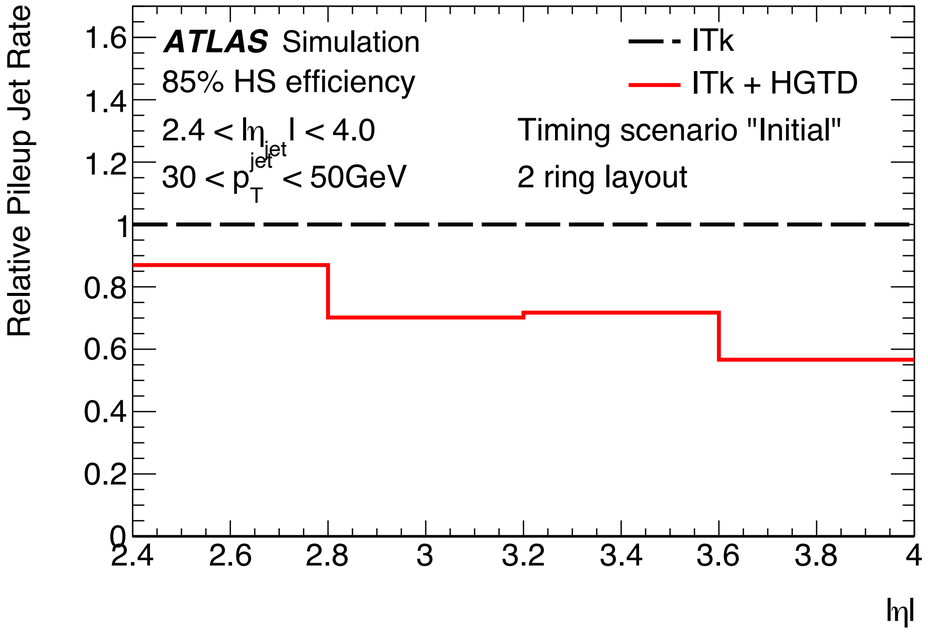


High Granularity Timing Detector

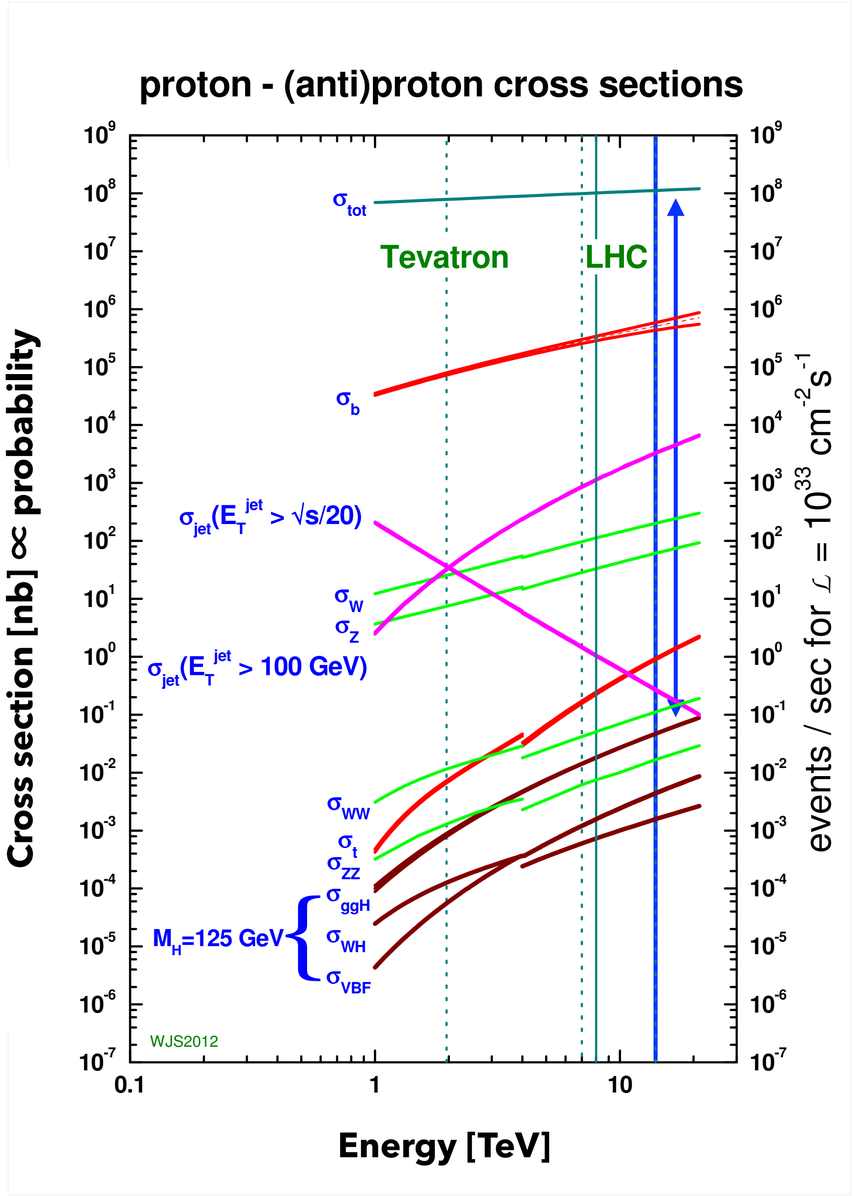
- Precision time reconstruction (30 ps) with LGAD
- Coverage: 2.4 < |η| < 4.0
- Pixel size: 1.3 x 1.3 mm², thickness: 50 μm
- Improved pileup jet suppression







Cross Section and Trigger

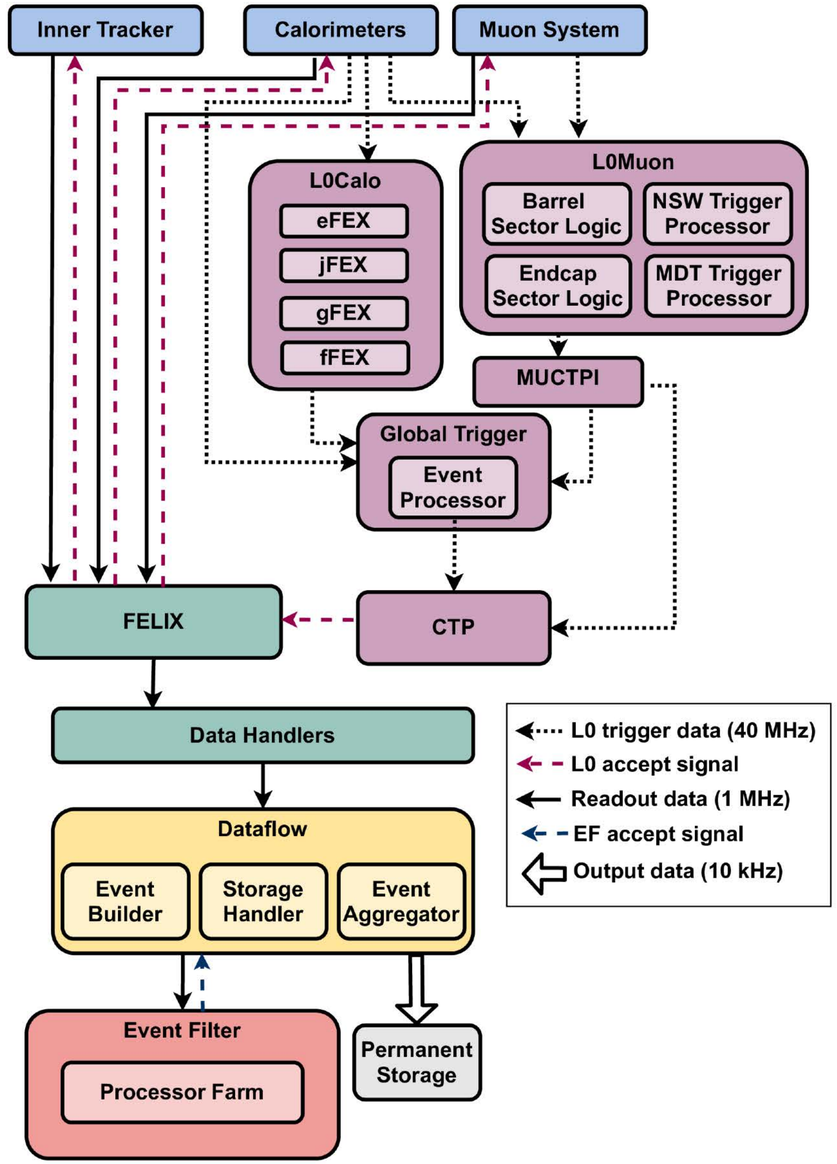


The cross section of the Higgs boson production is only 0.0000000005 of the total cross section of the proton-proton collision…

We select interesting collisions before storage — “trigger”.

Trigger and DAQ Upgrade

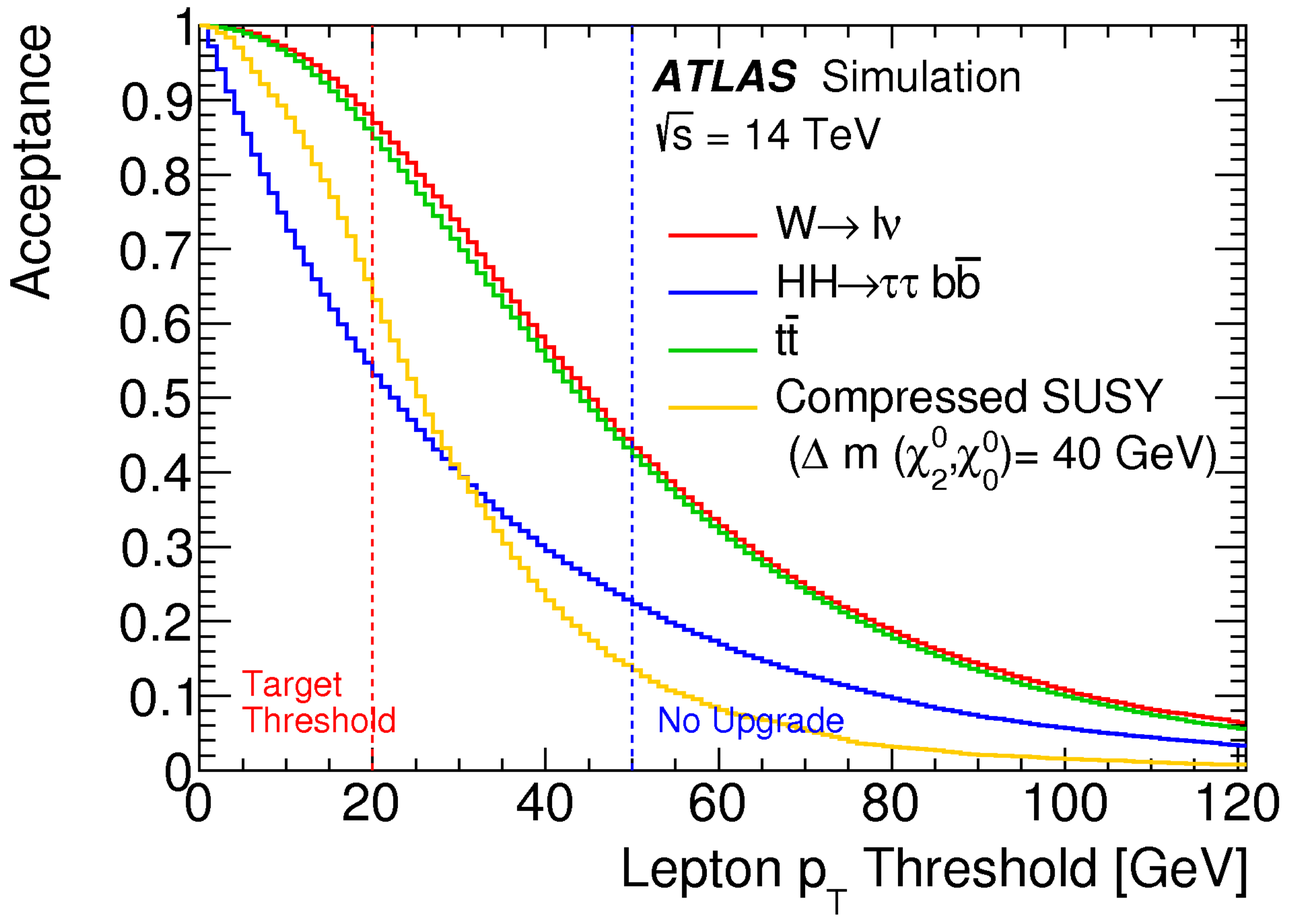
- Level 0: 1 MHz, ~5.2 TB/s, latency 10 μs
  - LHC: 100 kHz, ~290 GB/s, latency 2.5 μs
- Event Farm: 10 kHz, ~52 GB/s
  - LHC: 1 kHz, ~2.9 GB/s



Trigger and DAQ Upgrade

With the upgrade of the trigger and DAQ system, trigger thresholds similar to those used at Run I can be used at HL-LHC.

Retain high acceptance for various physics processes!

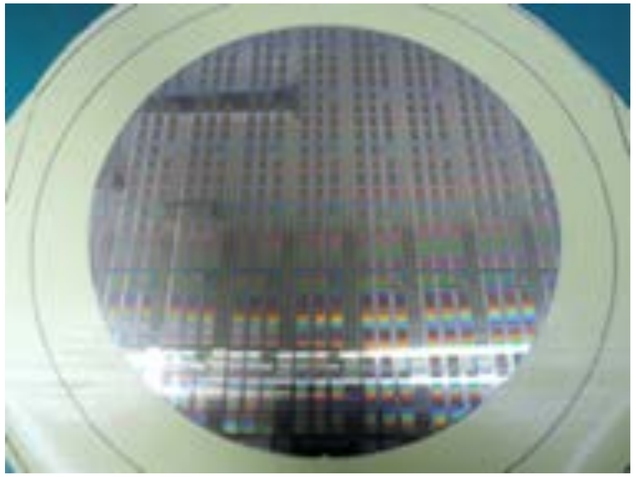


TGC System for HL-LHC

	Numbers
Detector channels	320k
ASD boards	23k
PS boards	1434
JATHub boards	148
SL borads	48

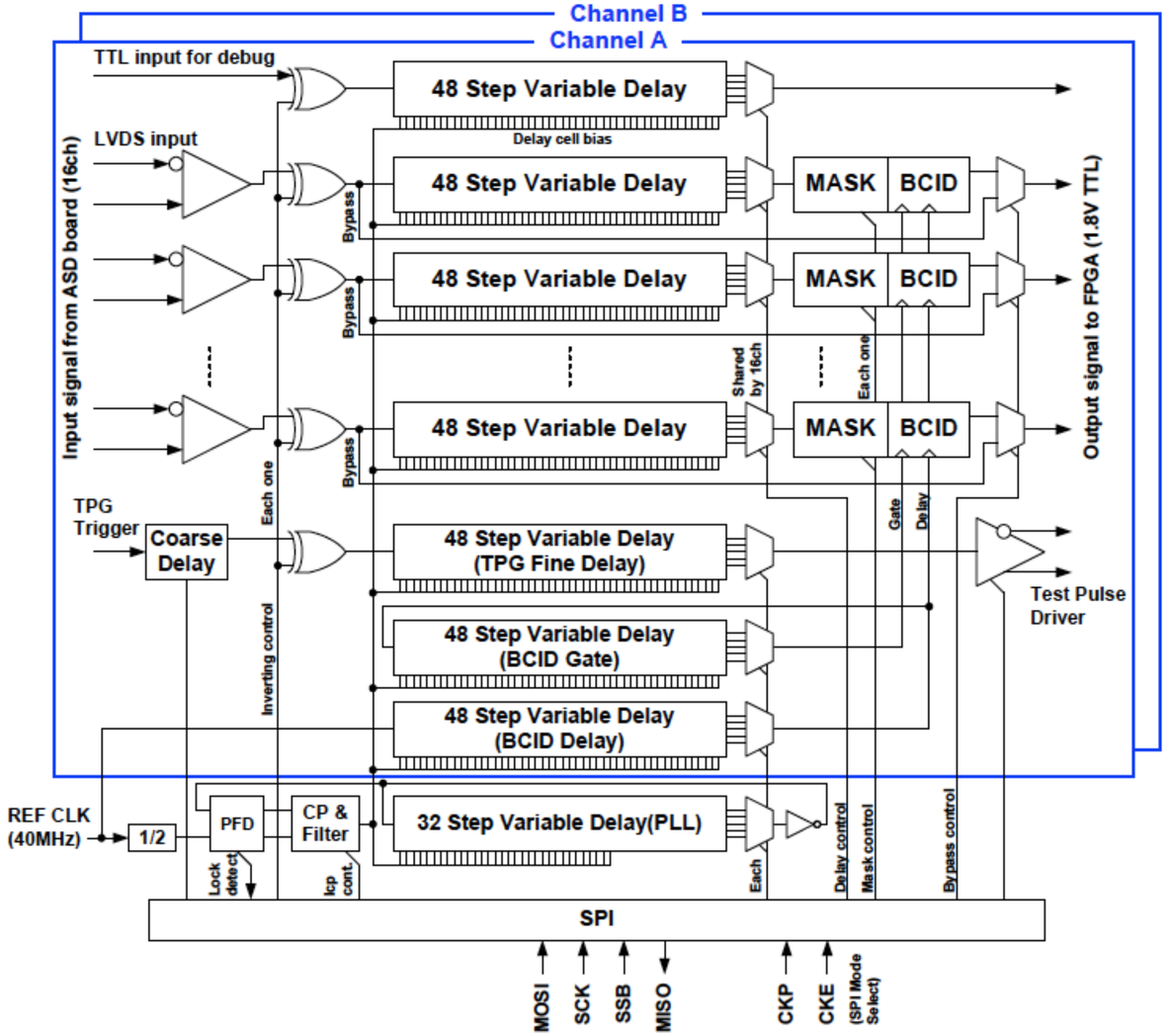
} Newly developed

PP ASIC





Design process	Silterra 0.18 μs CMOS 6M1P
Supply voltage	3.3 V (LVDS Rx, TPG Driver) 1.8 V (PLL, Delay line, CMOS input and output) Voltage tolerance : ± 10 %
# of channels	Group A (16 ch), Group B (16 ch)
Timing control resolution	< 1 ns
Timing control range	> 40 ns
Timing jitter	~40 ps (LVDS Rx), ~40 ps (Variable Delay)
Temperature range	0 ~ 80 ℃
Power consumption	~20 mW (Previous design: 130 mW)



PS Board — Challenge

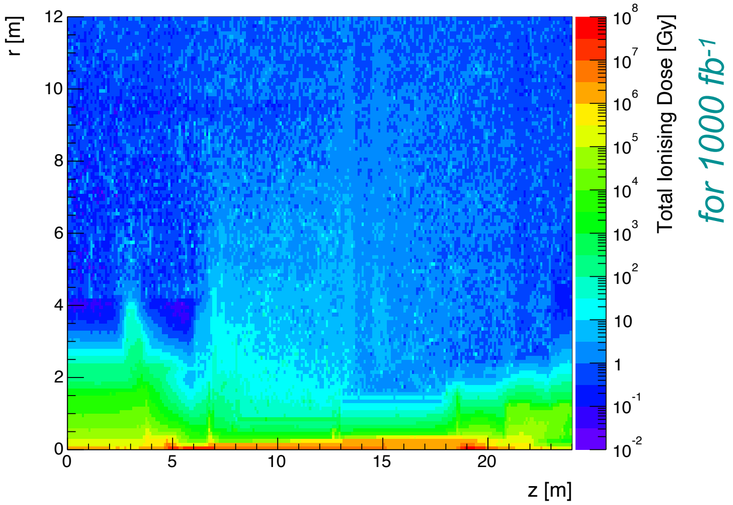
In order to establish a robust system, we use commercial-off-the-shelf (COTS) products for PS boards wherever possible.

Challenge: confirmation of the radiation tolerance of COTS products!

Simulation of radiation level

(Total Ionising Dose, TID)

PS board: 6 Gy at HL-LHC



Safety factors

- SF_{sim}: safety factor for simulation uncertainty
- SF_{ldr}: safety factor for low-dose rate at actual experiment
- SF_{lot}: safety factor for lot-to-lot difference and difference in lot

SF_{sim}			SF_{ldr}				SF_{lot}	
TID	NIEL	SEE	TID (COTS)	TID (ASICs)	NIEL	SEE	All (COTS)	All (ASICs)
1.5	2	2	1–5	1–1.5	1	1	1–4	1–2

Example: SF for FPGA TID: 1.5 x 5 x 4 = 30, requirement: 180 Gy

SL Board — Prototyping

First prototype tested:

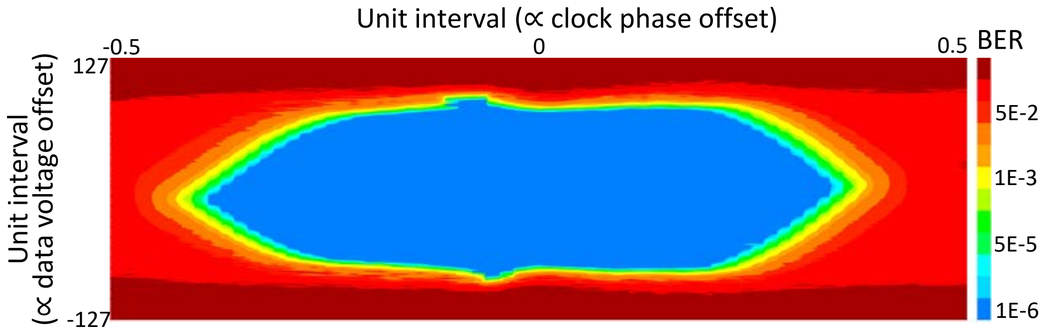
- Power up/down sequencing
- Temperature monitoring
- FPGA configuration and initial trigger firmware test
- FireFly loopback
- MPSoC-FPGA connection
- IMPC-Shelf manager connection
- Clock recovery for fixed latency (zero delay mode of Si5345)

Second prototype development in 2023

TWEPP 2022

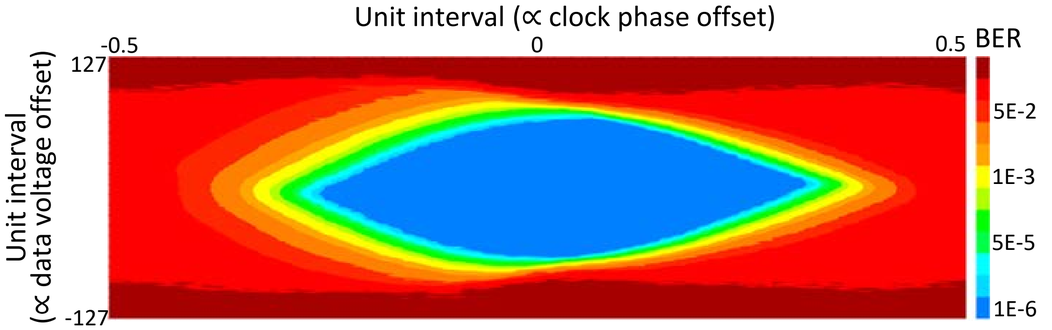
Result of FireFly loopback test with Xilinx IBERT

9.6 Gb/s assumed max rate for SL



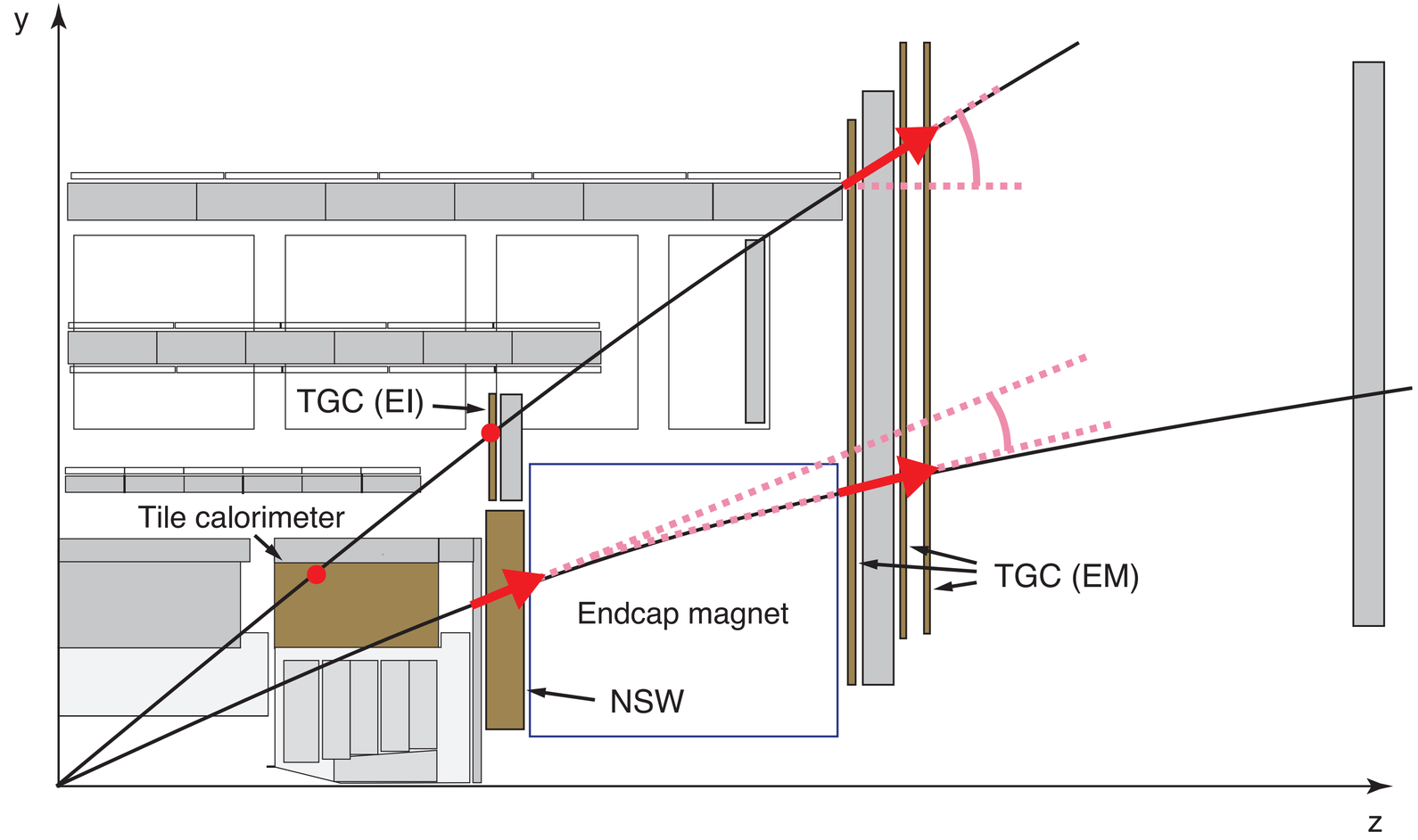
Nominal point (dedicated measurement):
BER < 3.4×10^{-15} (95 % C.L.)

18.0 Gb/s as a test of board capacity



$$\text{BER (Bit Error Ratio)} = \frac{\text{Number of error bits}}{\text{Number of transferred bits}}$$

Fast Muon Reconstruction — Design



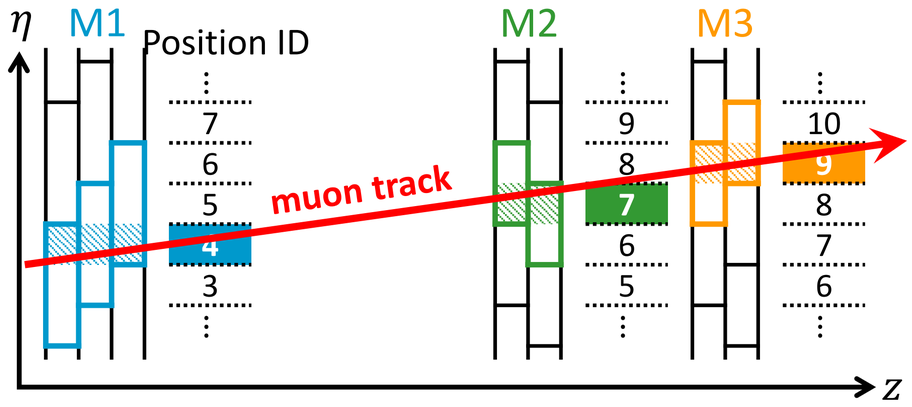
Muon tracks reconstructed from TGC (EM) and selected with inner detectors.

Fast Muon Reconstruction — Firmware

Pattern matching — ultimate method (concept: M. Tomoto, firmware design: Y. Horii)

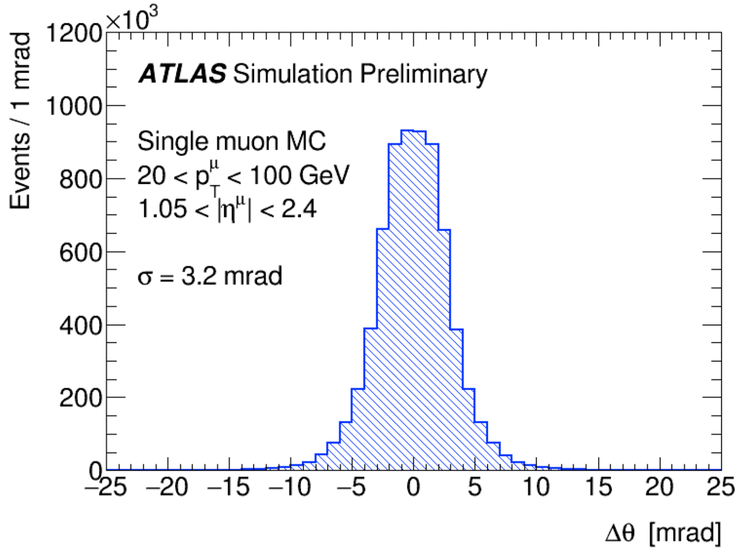
①Take coincidence and output position IDs in each of three stations: M1 (3 layers), M2 (2 layers) and M3 (2 layers)

②Combine position IDs on three stations and obtain segment data from FPGA UltraRAM where segment data are stored



Hit pattern list stored in UltraRAM

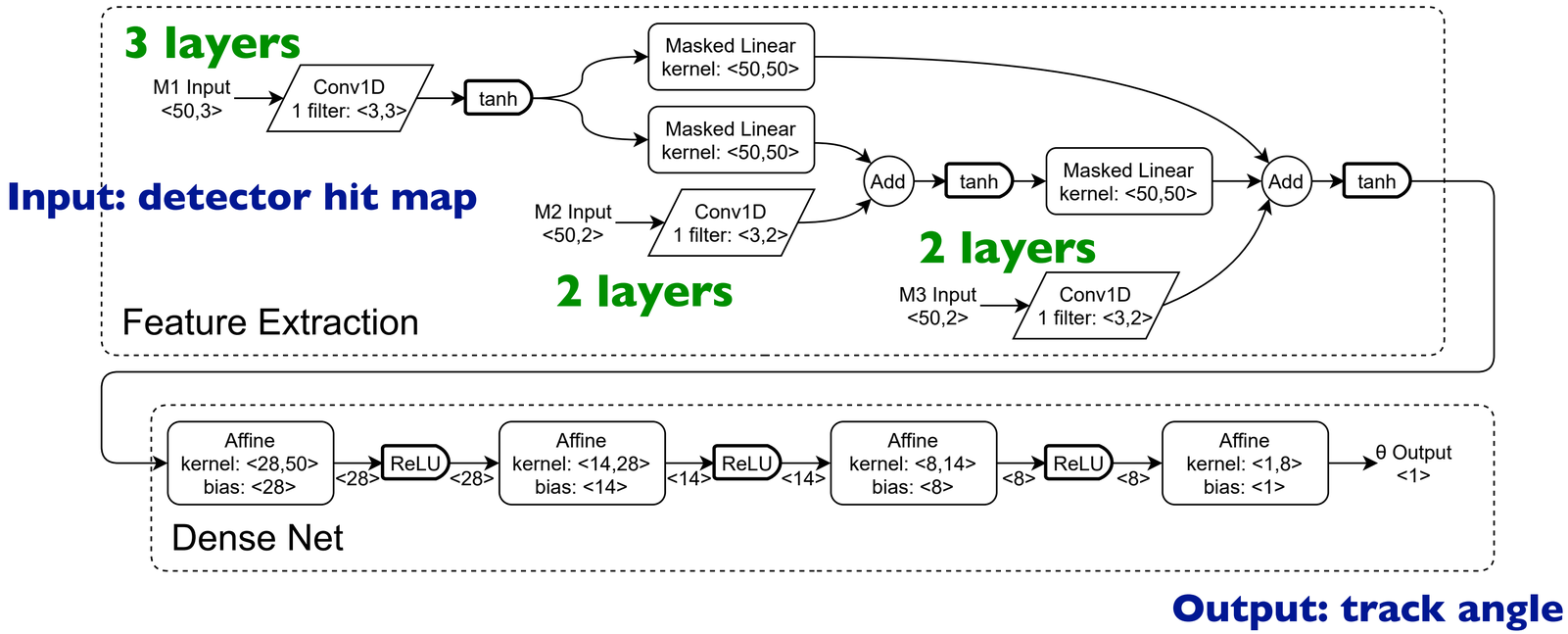
Position ID			Track segment (position, angle)
M1	M2	M3	
4	7	8	η_1, θ_1
4	**7**	**9**	$\boldsymbol{\eta_2, \theta_2}$
4	7	10	η_3, θ_3

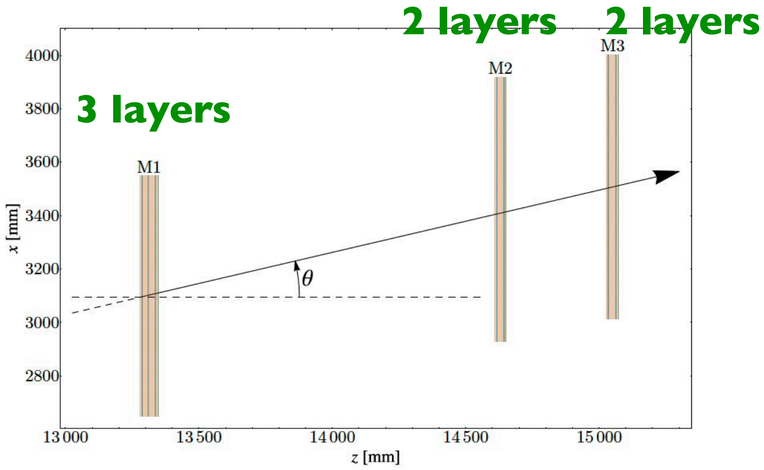


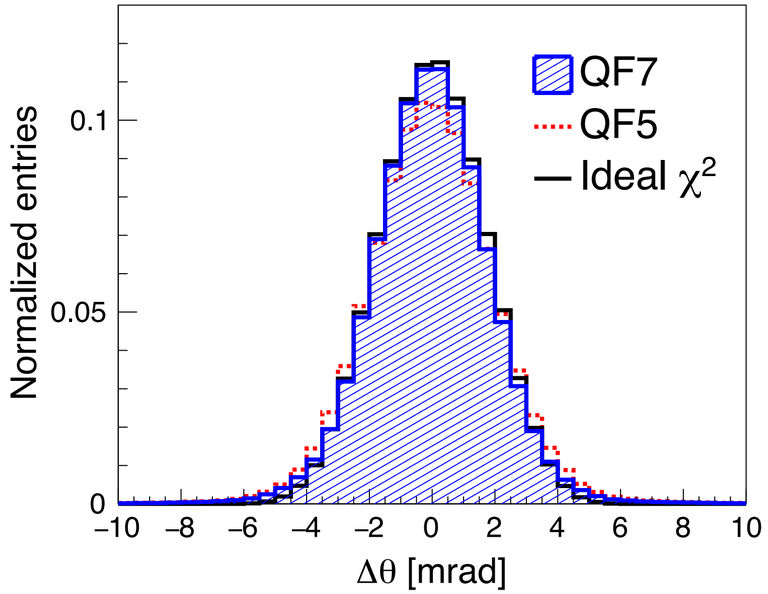
https://twiki.cern.ch/twiki/bin/view/AtlasPublic/L0MuonTriggerPublicResults#Performance_of_trigger_algorithm

Fast Muon Reconstruction — New Method

Compact CNN — structure optimised for the TGCdetector, quantised parameters, sparse network



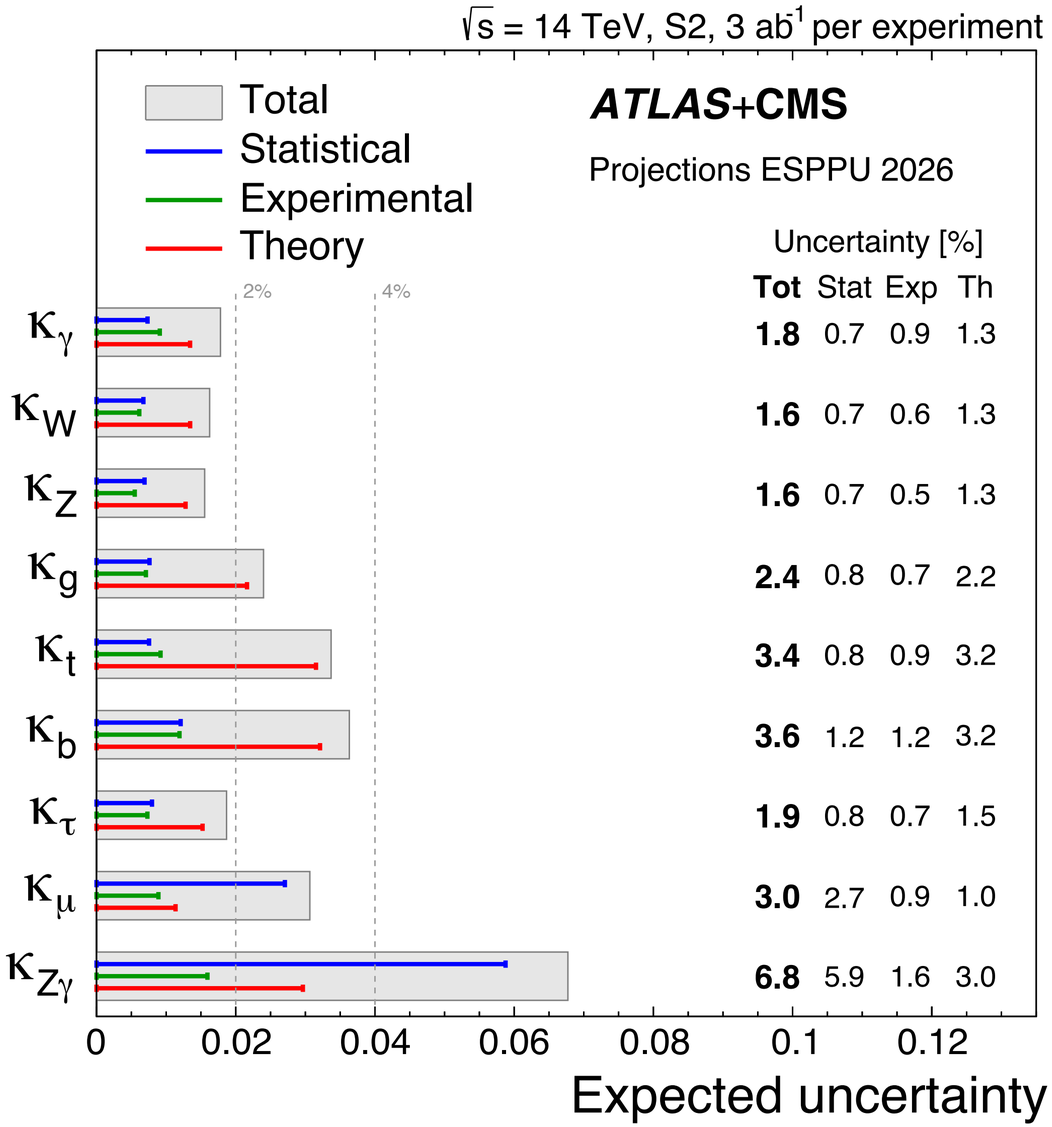




Successfully implemented in XCVU13P FPGA, latency < 100 ns

[NIMA 1045, 167546 (2023)]

Higgs Coupling at HL-LHC



A few % for various couplings!

Deviation from the SM

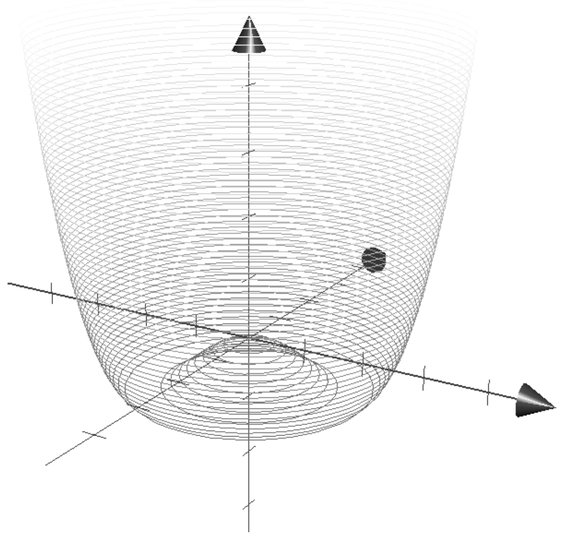
— indication of BSM

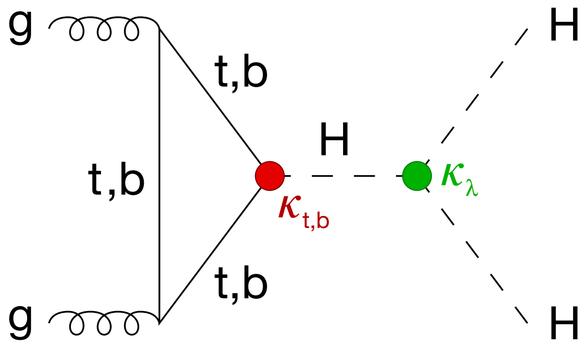
Consistency with the SM

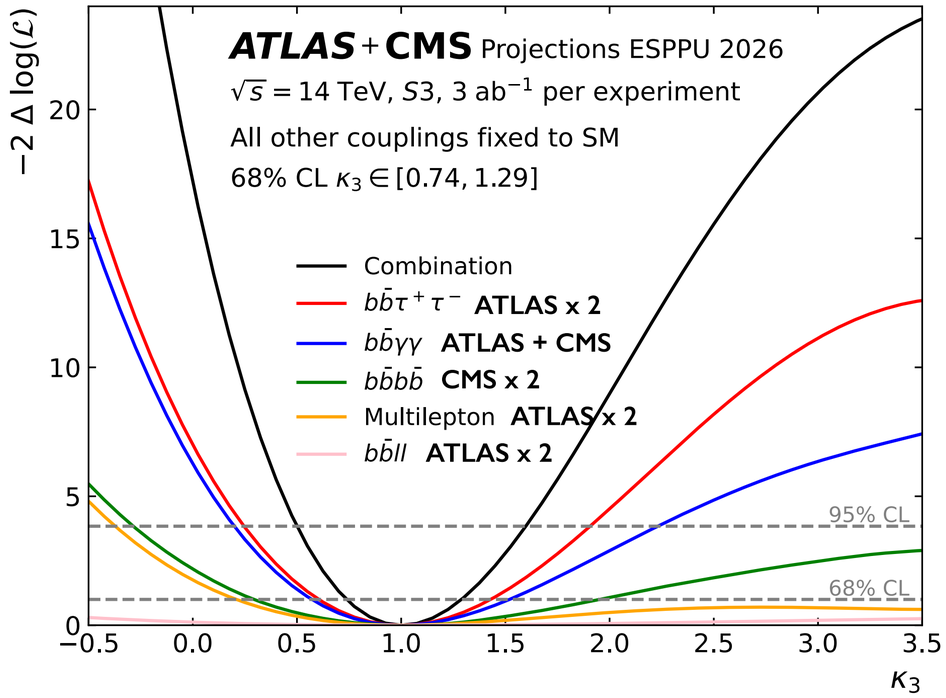
— stringent constraint on BSM

Di-Higgs Search at HL-LHC

Non-resonant HH production sensitive to Higgs self-coupling λ







$$V(\phi) = -\mu^2\phi^\dagger\phi + \lambda(\phi^\dagger\phi)^2$$

$$\phi = \sqrt{\frac{1}{2}}\begin{pmatrix} 0 \\ v + H(x) \end{pmatrix}$$

Uncertainty on κ_λ: −26%/+29%