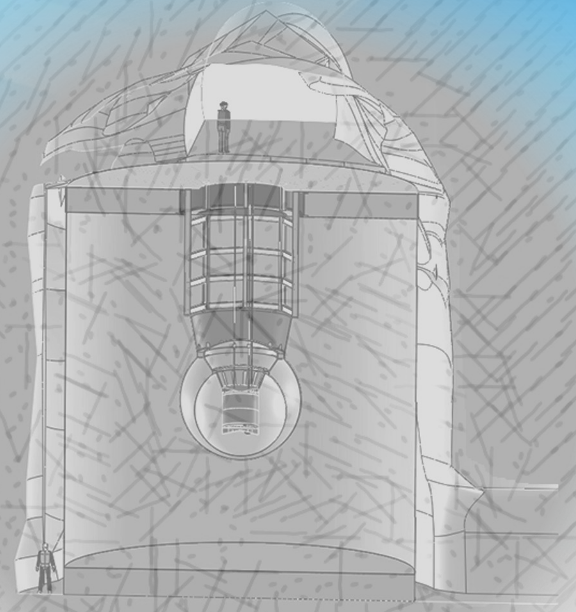


Ionization readout in nEXO using liquid xenon submerged CRYO ASIC

Evan Angelico, on behalf of the nEXO collaboration

Nagoya Workshop, Feb 16th, 2024

Observing lepton number violation and a new class of particle, the Majorana Fermion

nEXO

diagrams from André de Gouvêa, lecture CENPA, Jan 16 2020

- Neutrinos have mass - major recent discovery, is not expected in standard model Higgs mechanism; how and why?
- Can boost to the rest frame of a neutrino, and flip its helicity
- Makes it possible for neutrinos to be Majorana Fermions
- Majorana implies lepton number violation, matter/antimatter asymmetry problem in the observed universe

$$\nu_L \leftarrow \mathrm{CP} \rightarrow \bar{\nu}_R$$
$$\updownarrow \text{“Lorentz”}$$
$$\nu_R \leftarrow \mathrm{CP} \rightarrow \bar{\nu}_L$$

Dirac neutrino

$$\nu_L \leftarrow \mathrm{CP} \rightarrow \nu_R$$
$$\updownarrow \text{“Lorentz”}$$
$$\nu_R \leftarrow \mathrm{CP} \rightarrow \nu_L$$

Majorana neutrino

Observing lepton number violation and a new class of particle, the Majorana Fermion

- Neutrinos have mass - major recent discovery, is not expected in standard model Higgs mechanism; how and why?
- Can boost to a rest frame of a neutrino, and flip its helicity
- Makes it possible for neutrinos to be Majorana Fermions
- Majorana implies lepton number violation, matter/antimatter asymmetry problem in the observed universe

<u>Regardless of the outcome, measuring the Majorana nature of the neutrino has groundbreaking implications</u>

The neutrino has a **non-zero Majorana mass**: additional physics beyond the standard model

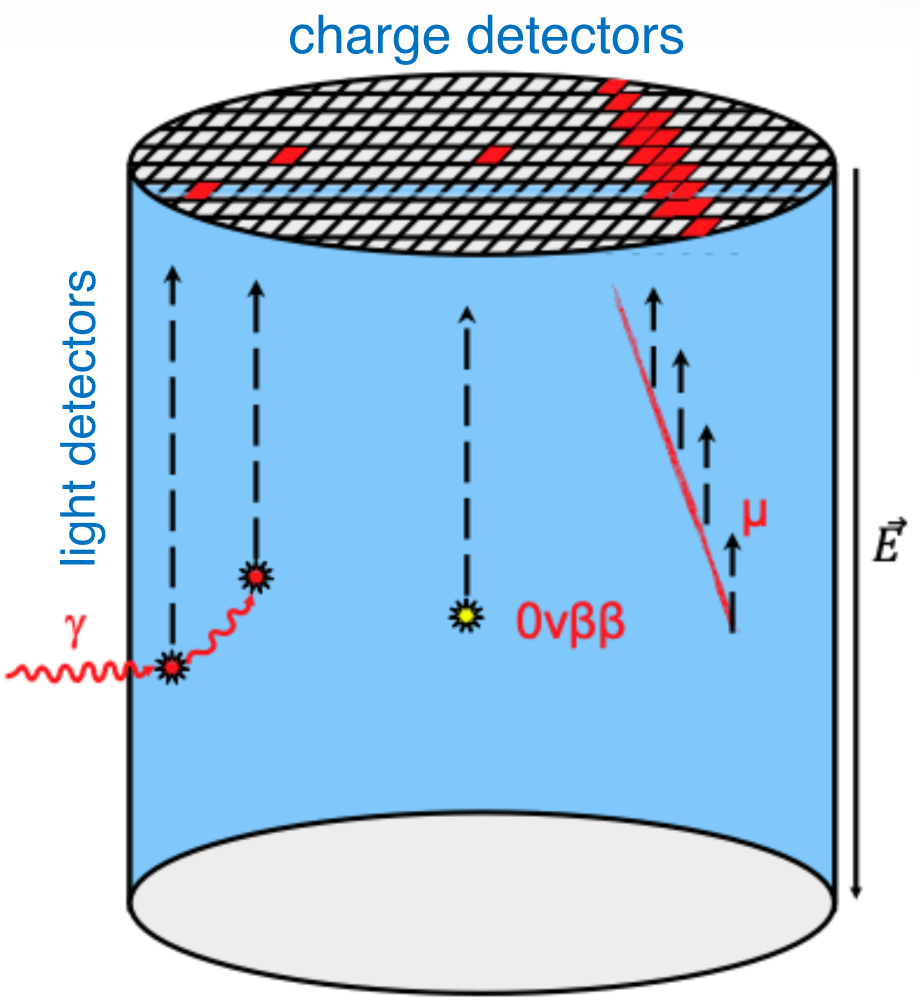
The neutrino has **zero Majorana mass**: lepton number is conserved, why is lepton number special physically?

Liquid ^{136}Xe time projection chamber

nEXO

Single phase liquid xenon (enriched in $0\nu\beta\beta$ isotope) is an excellent technology for detecting $0\nu\beta\beta$

nEXO is a single phase, 5000 kg TPC enriched to 90% in ^{136}Xe



What are some main differences between constraints for $0\nu\beta\beta$ verses WIMP DM in LXe?

Energy and number of quanta

Energy of $0\nu\beta\beta$ is 2.458 MeV into two electrons

with 400 V/cm field in the drift region

140,000 electrons in a 3-mm 3σ “diameter” cloud

Energy and number of quanta

nEXO

Energy of $0\nu\beta\beta$ is 2.458 MeV into two electrons

with 400 V/cm field in the drift region

140,000 electrons in a 3-mm 3σ “diameter” cloud

- plenty for detecting with a solid-state amplifier
- nEXO is a single phase TPC with no “S2” amplification

Radioactive backgrounds

2.458 MeV has overlap with naturally occurring radioactive nuclei that produce gammas

Other backgrounds, such as alpha emitters, are identifiable by light-charge anti-correlation

nEXO has multiple strategies for (1) controlling radioactive background levels and (2) distinguishing $0\nu\beta\beta$ from backgrounds

Radioactive backgrounds

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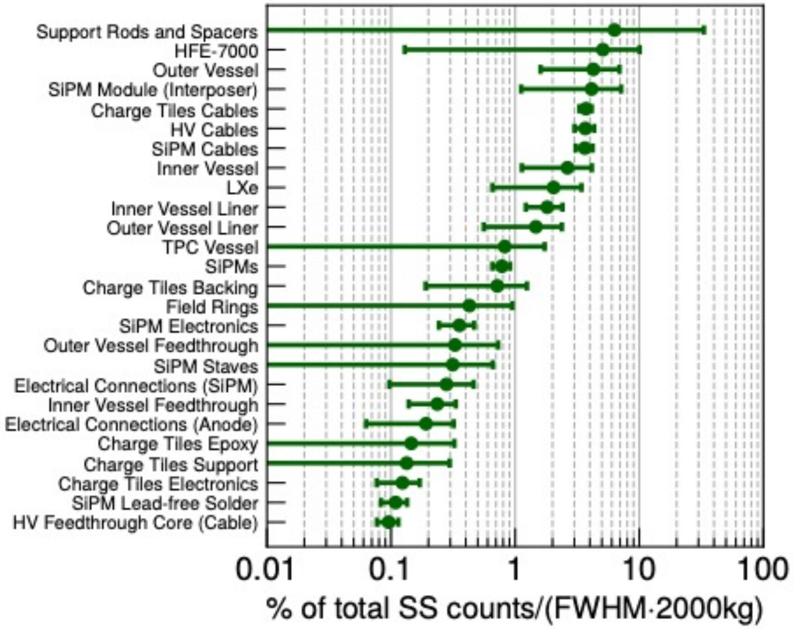


Assay every single material and component that goes into nEXO

Radioactive backgrounds

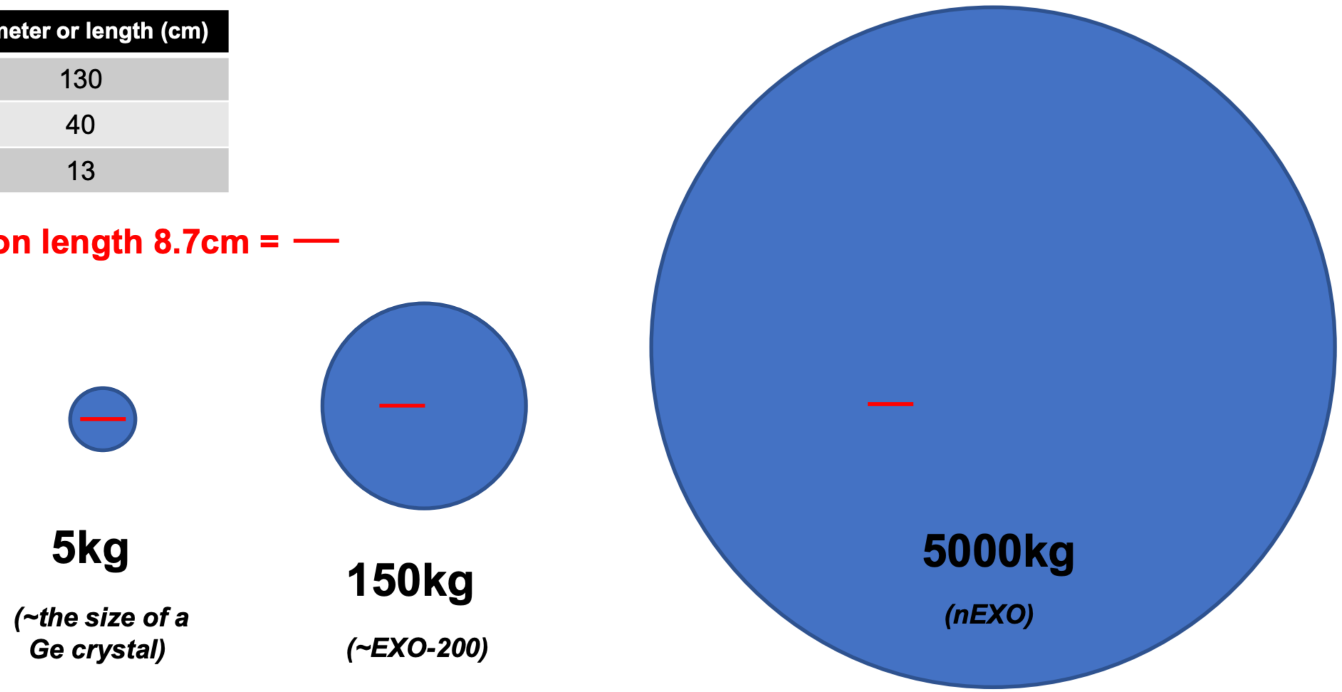
2.458 MeV has overlap with naturally occurring radioactive nuclei that produce gammas

Other backgrounds, such as alpha emitters, are identifiable by light-charge anti-correlation

nEXO has multiple strategies for (1) controlling radioactive background levels and (2) distinguishing $0\nu\beta\beta$ from backgrounds

LXe mass (kg)	Diameter or length (cm)
5000	130
150	40
5	13

2.5 MeV γ attenuation length 8.7cm = —



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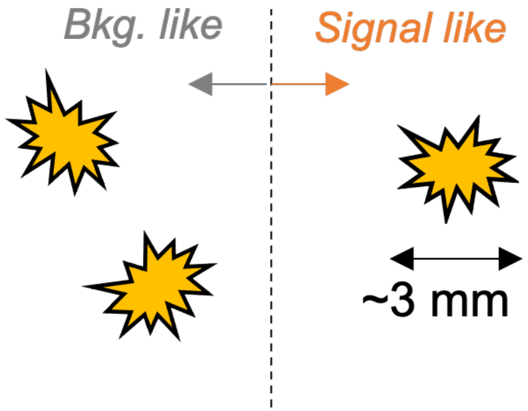
Topology:



Radioactive backgrounds

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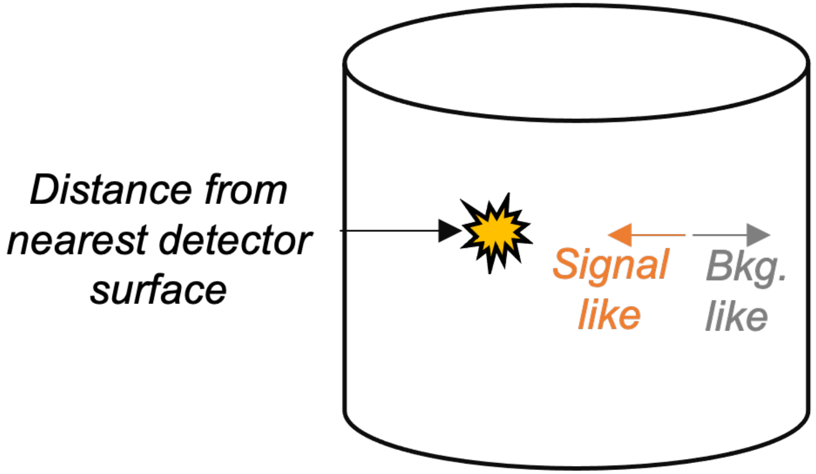
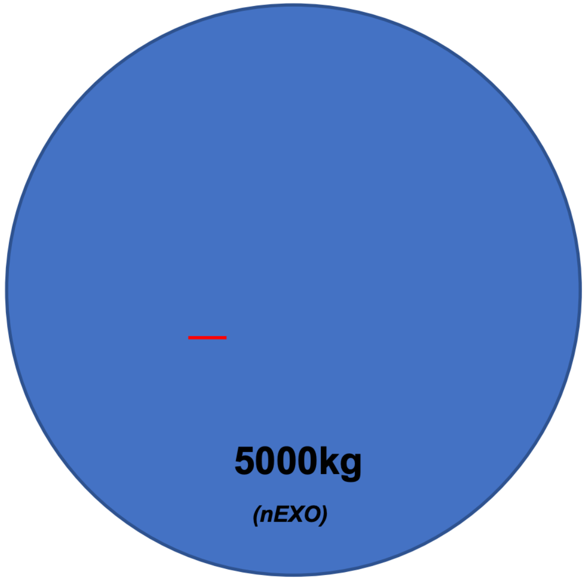
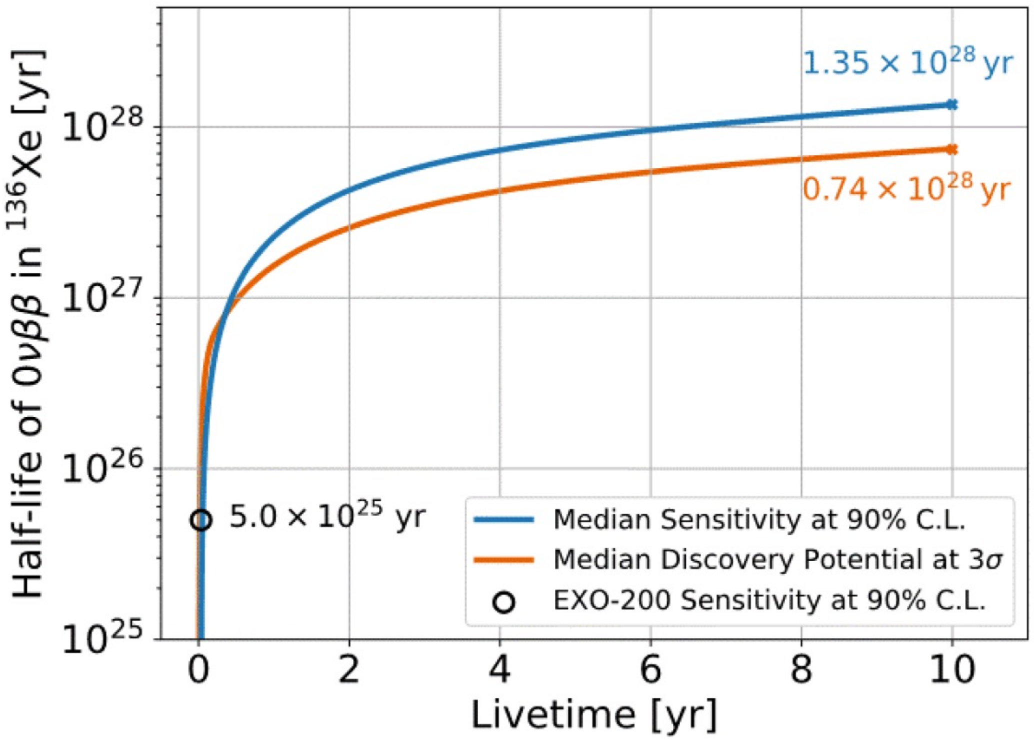
Standoff:

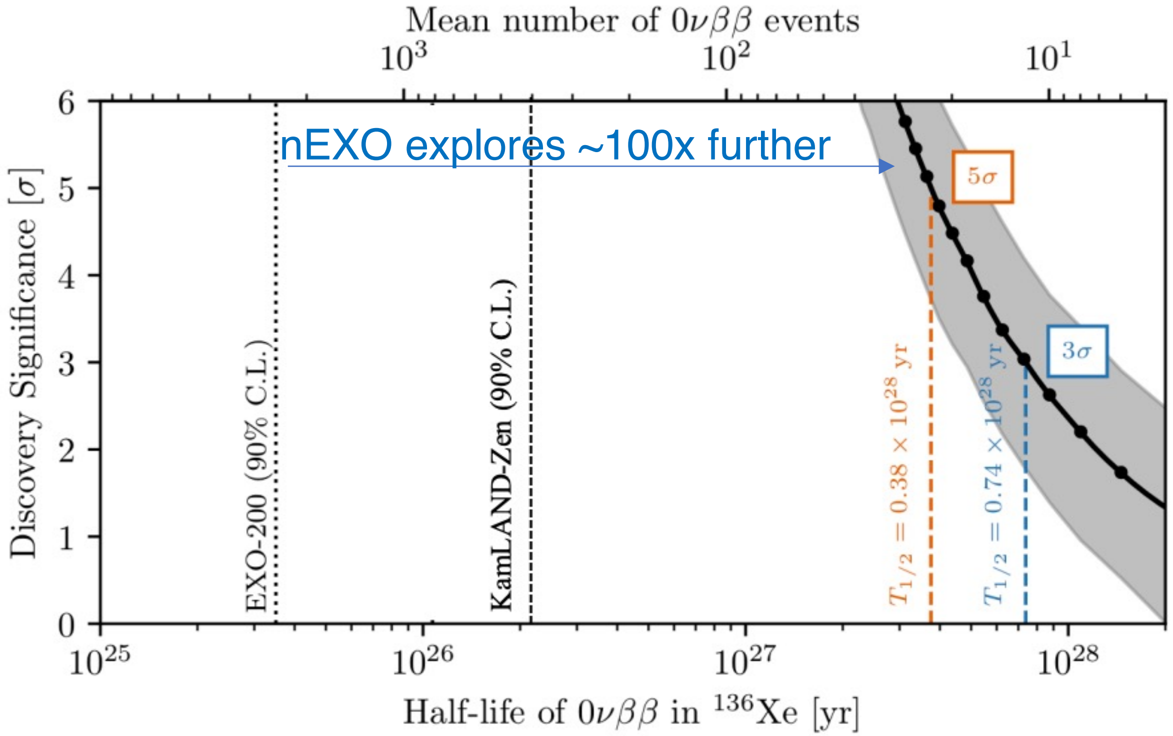




Projected sensitivity

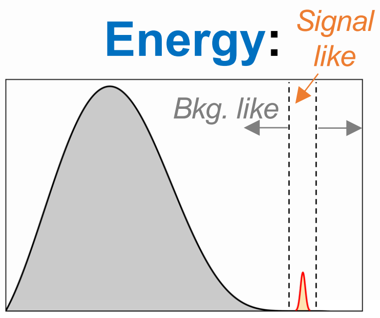
The measurable quantity of the experiment is the half-life of $0\nu\beta\beta$ in ^{136}Xe

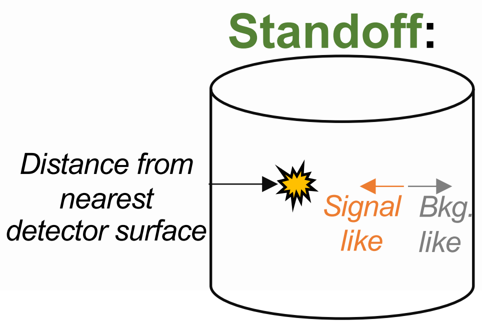


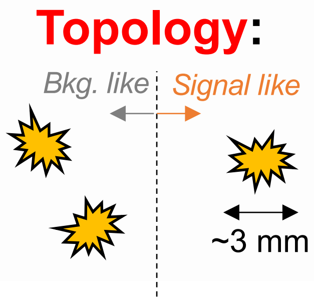


More details about the 0vbb reconstruction algorithm from these multiple parameters can be found at *J. Phys. G: Nucl. Part. Phys.* **49**, 015104 (2022)

Ionization charge detection influences each of the observables



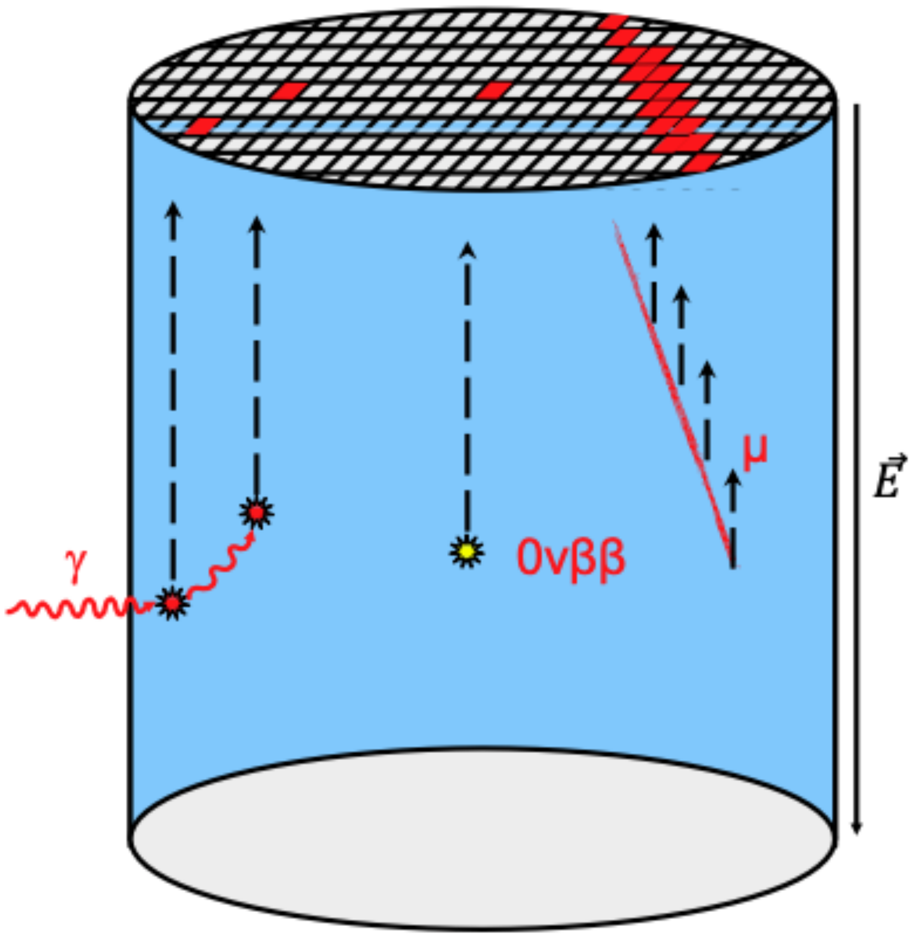




1. **Count charges** with <1% precision at Q-value (140,000 electrons)

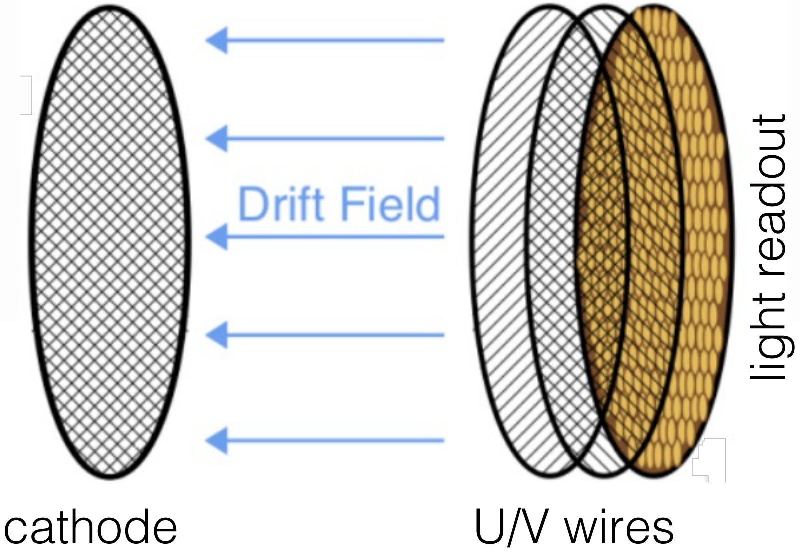
2. **Position resolution** to identify distance from materials, and depth to correct for electron lifetime from impurities

3. Pixel segmentation to **identify separate charge** depositions

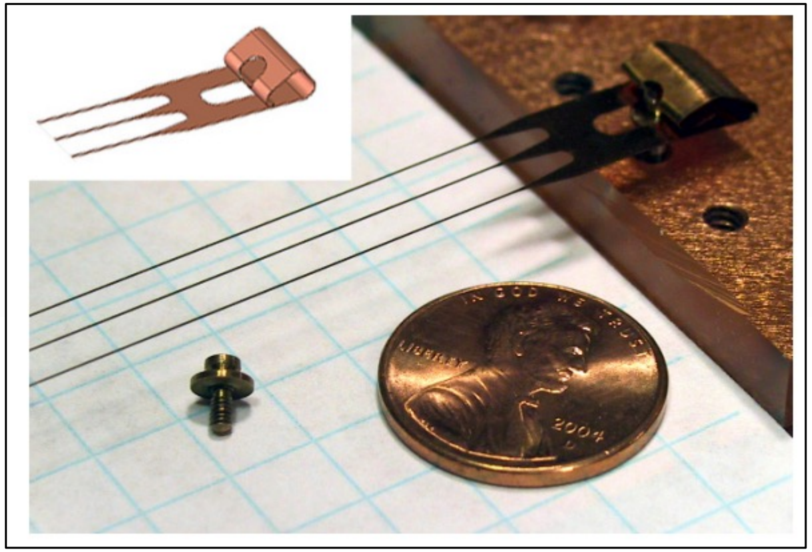


A modular charge collection "tile"

EXO-200 used wire planes for ionization detection



EXO-200 channel example, figure 8 from JINST 7 P05010, 2012

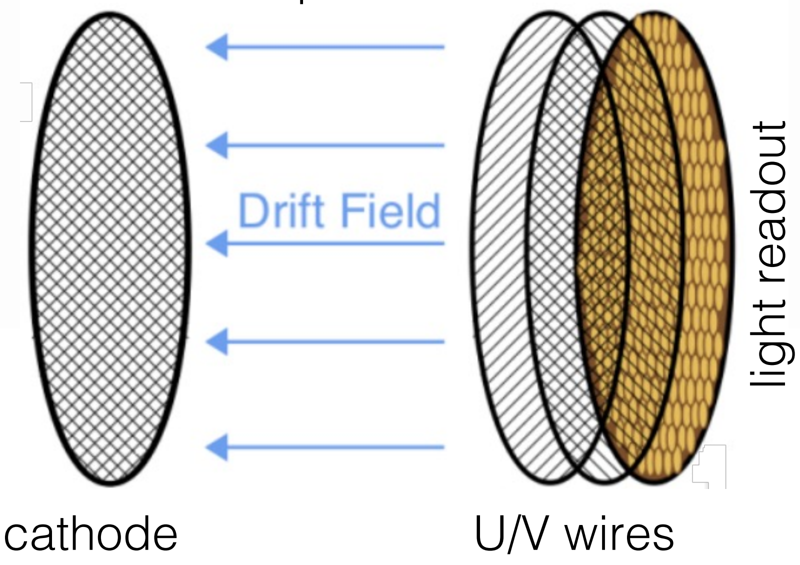


Some takeaways from the lessons about grids and wires at this workshop:

- R&D has been required for tensioning, deflection mitigation, and breakage mitigation
- Gets more difficult when scaling the area (1.2 m scale has been demonstrated well)
- (also has beneficial qualities)

A modular charge collection “tile”

EXO-200 used wire planes for ionization detection



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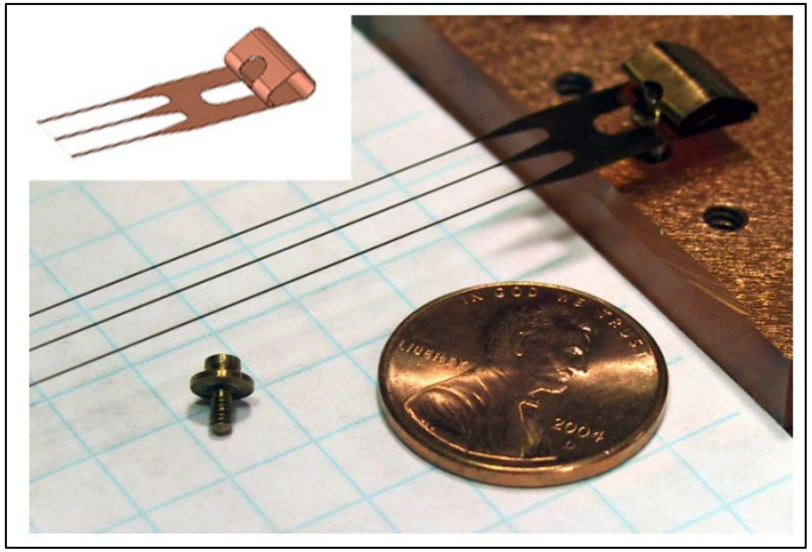
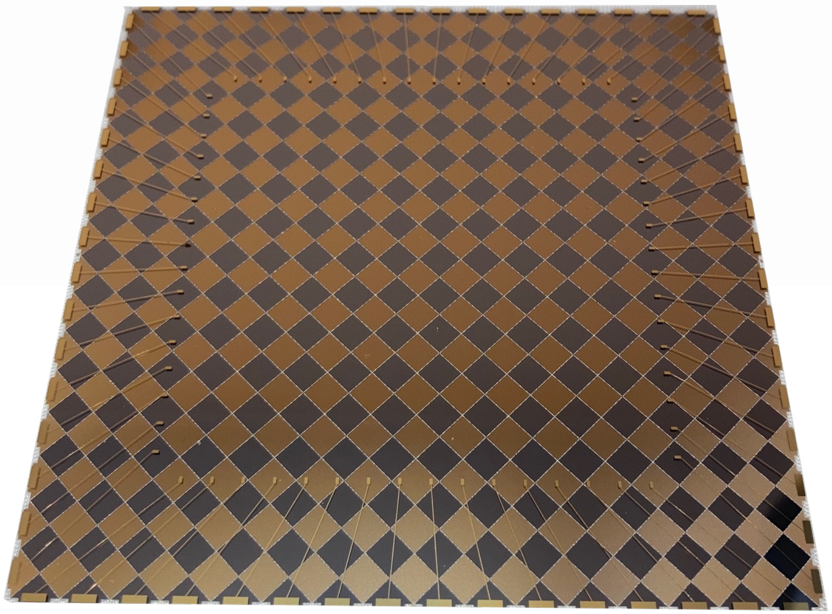


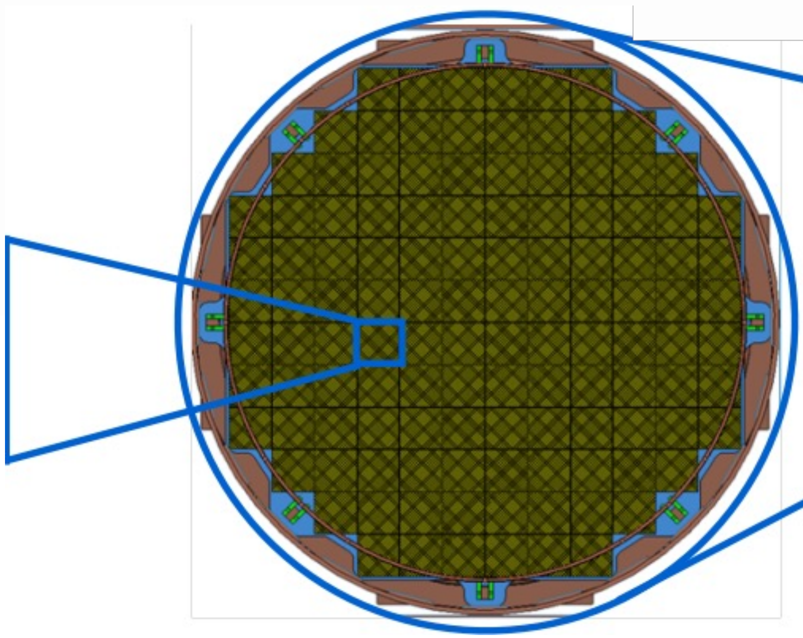
nEXO is, at the moment, grid and wire free:

- No need for extraction fields or Frisch grids
- Cathode is solid, monolithic electroformed copper

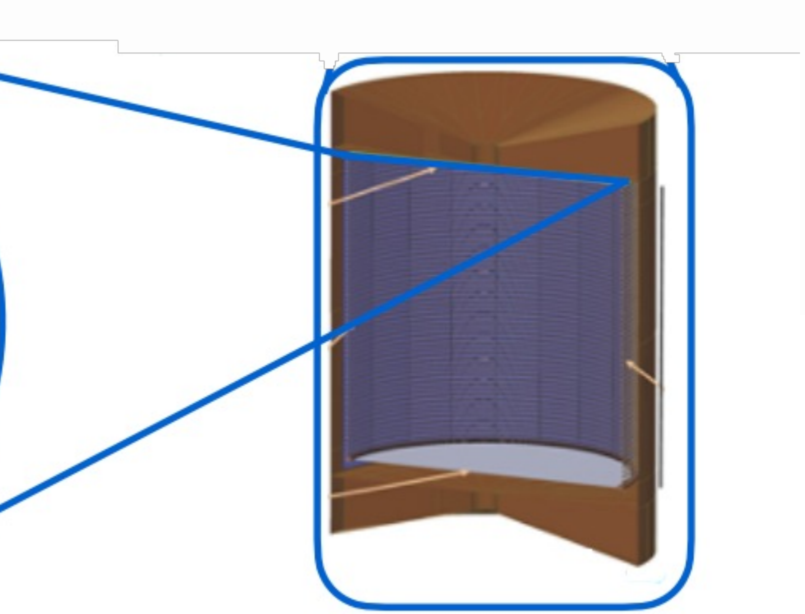
A modular charge collection “tile”



Vapor deposited electrode pattern on radiopure fused silica

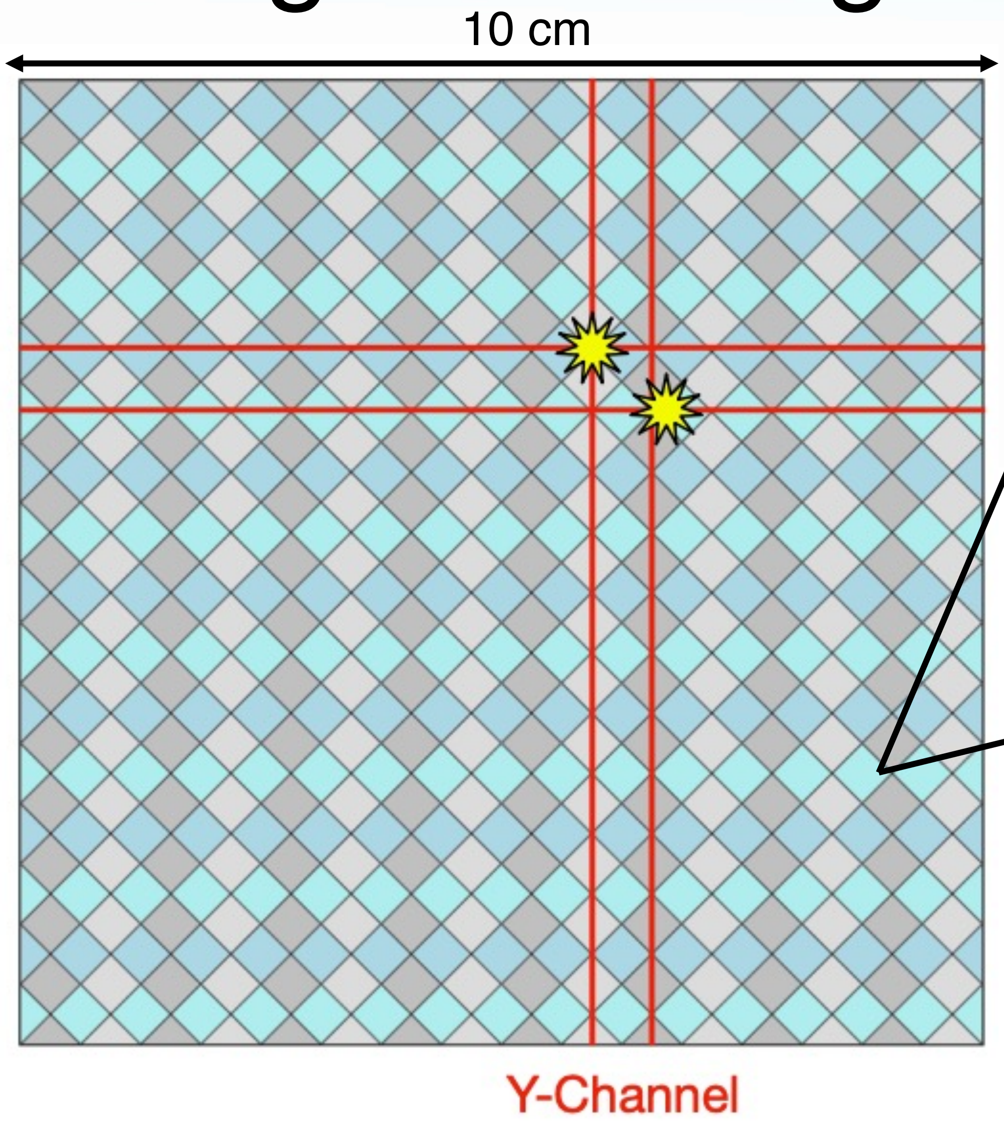


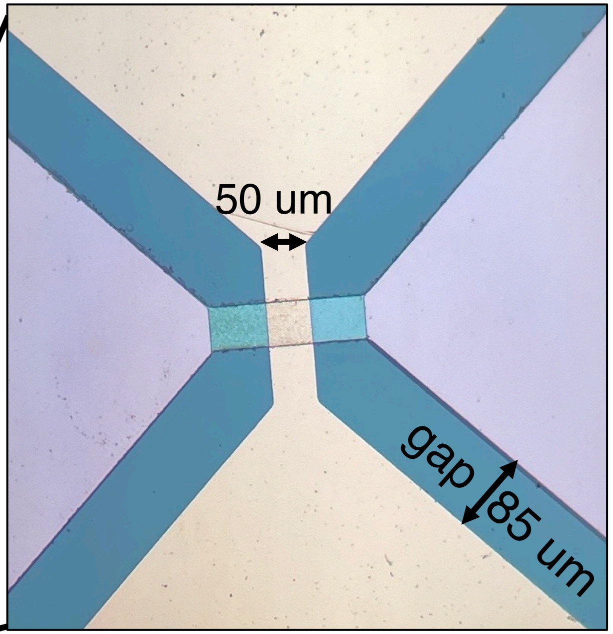
Tiled into an array of ~120 modules

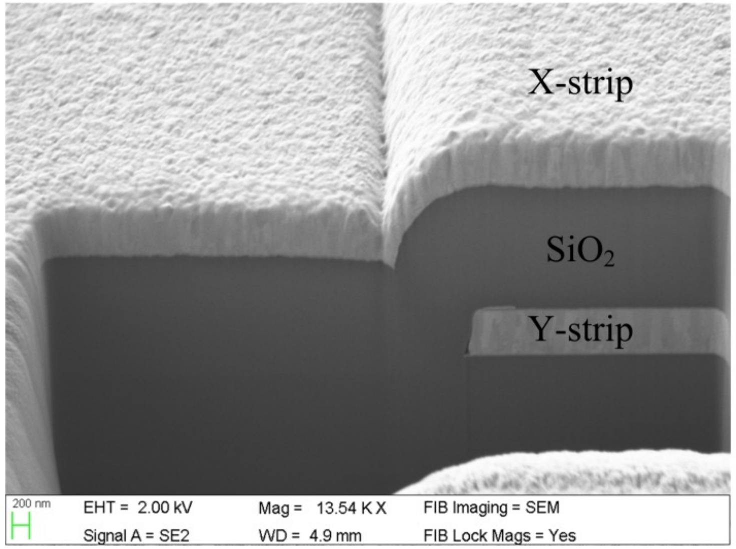


Forms the anode plane in nEXO TPC

Charge tile design and fabrication





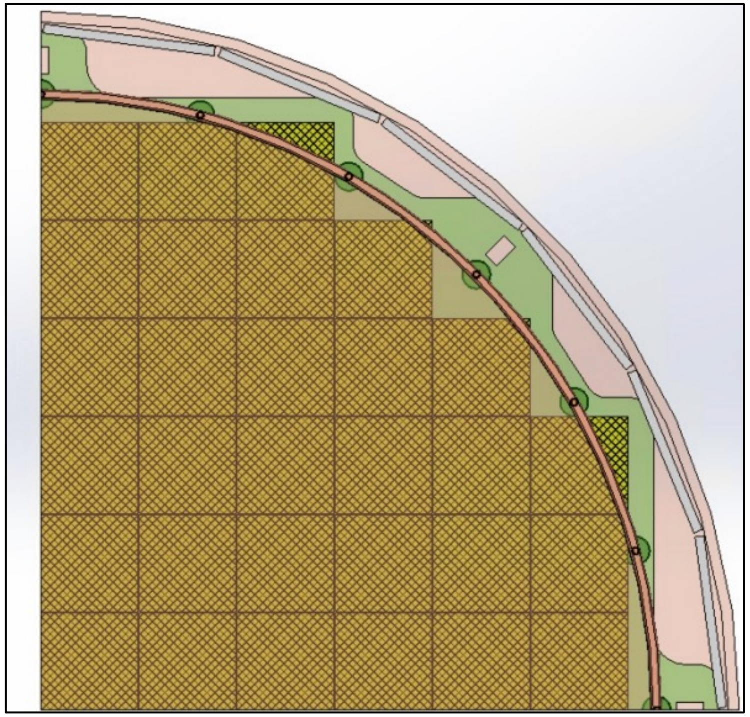


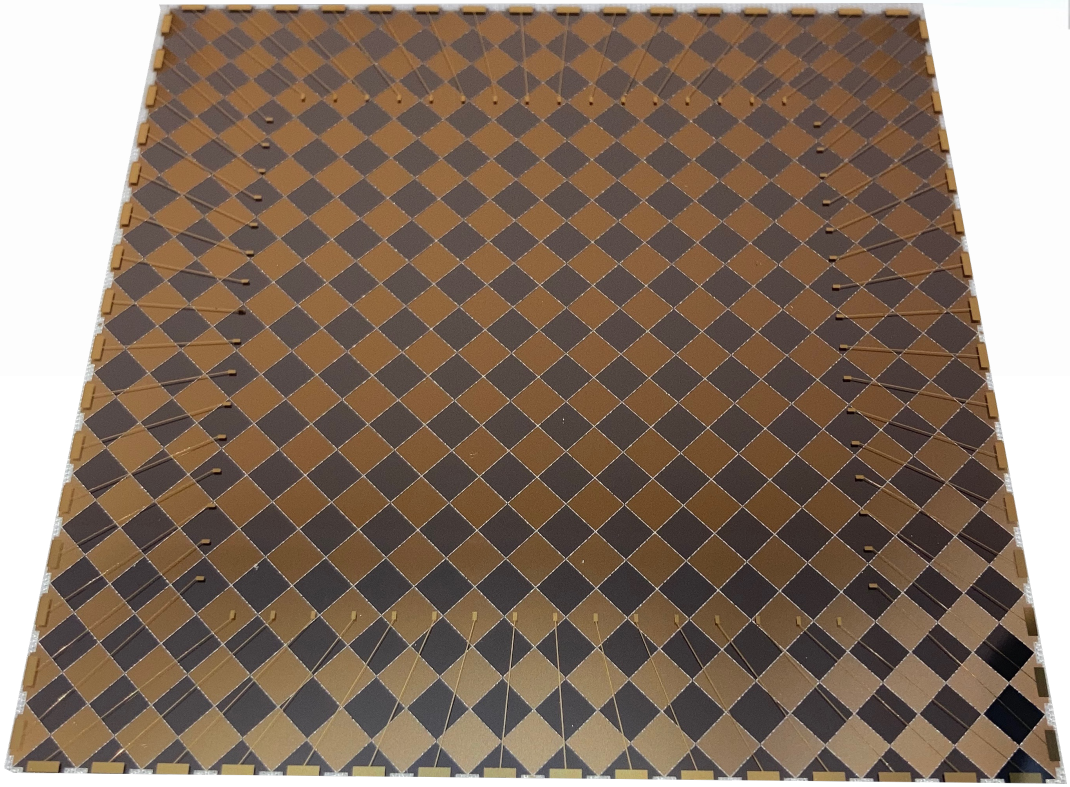
16 channels horizontal, 16 channels vertical = 32 channels

“crossings” occur where there is an insulating pad deposited

Charge tile design and fabrication

Tiles are arrayed side by side with little-to-no dead-space → Connections to electronics need to be on the back side



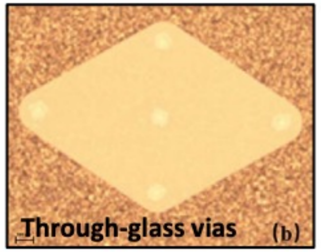


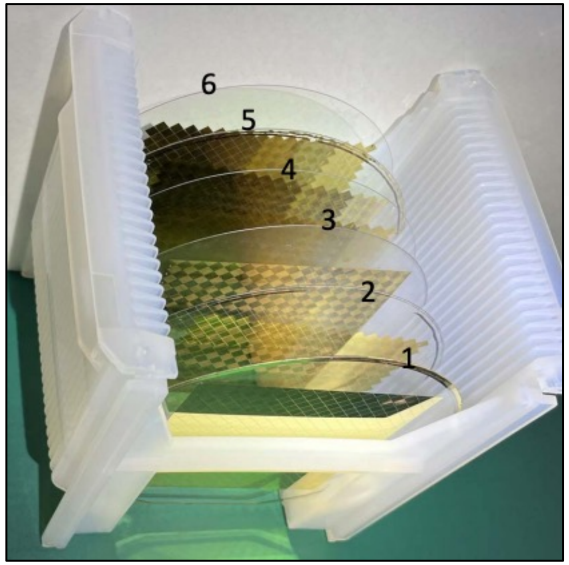
Radiopurity constraints require the tiles to be made of fused silica
how to get traces to the back side?

Two groups producing charge tiles

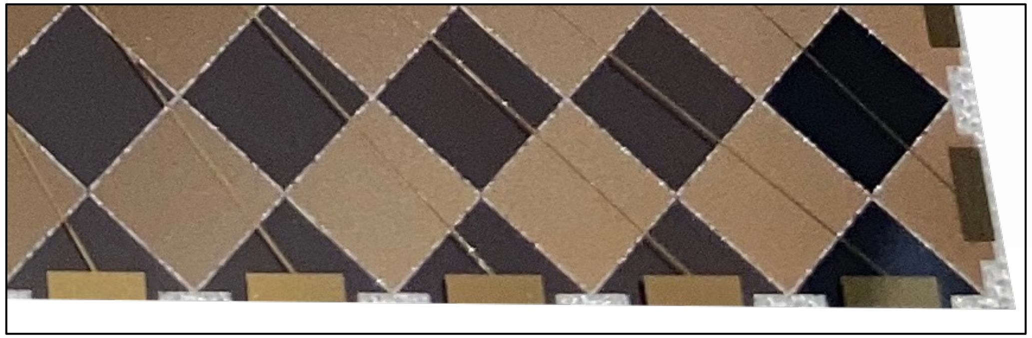
Institute of High Energy Physics (IHEP) - Institute of Microelectronics (IME)

Wu, X et al., *Electronics* (2023)





Stanford Linear Accelerator Center (SLAC)

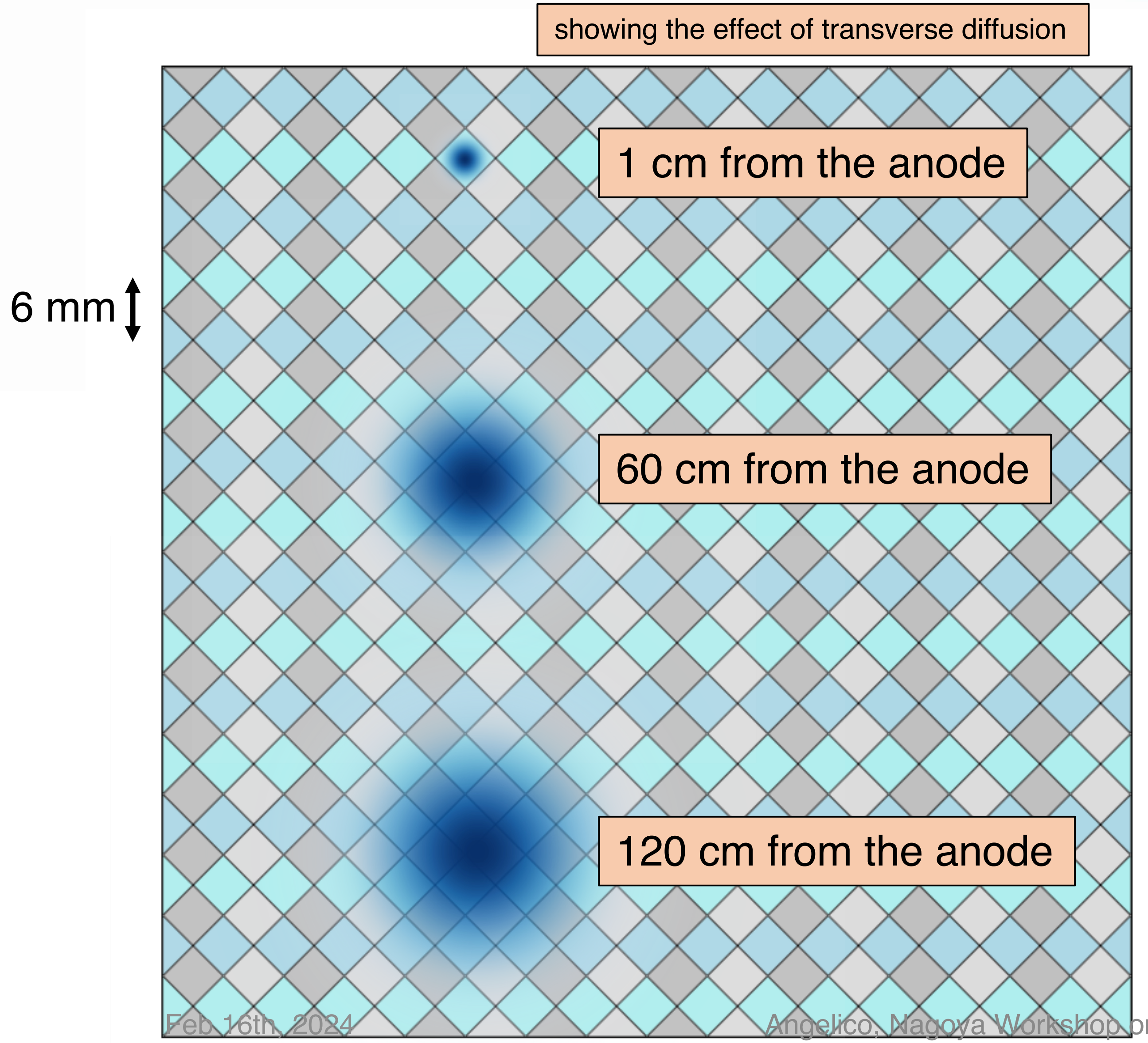


Strategies from both groups:
- Through fused silica vias
- Wraparound metalization at the edge

Challenges:
- Many depositions with processing chambers shared by many people

Both accomplishing front-to-back transition and electrode crossings; are producing prototypes

Charge tile design and fabrication



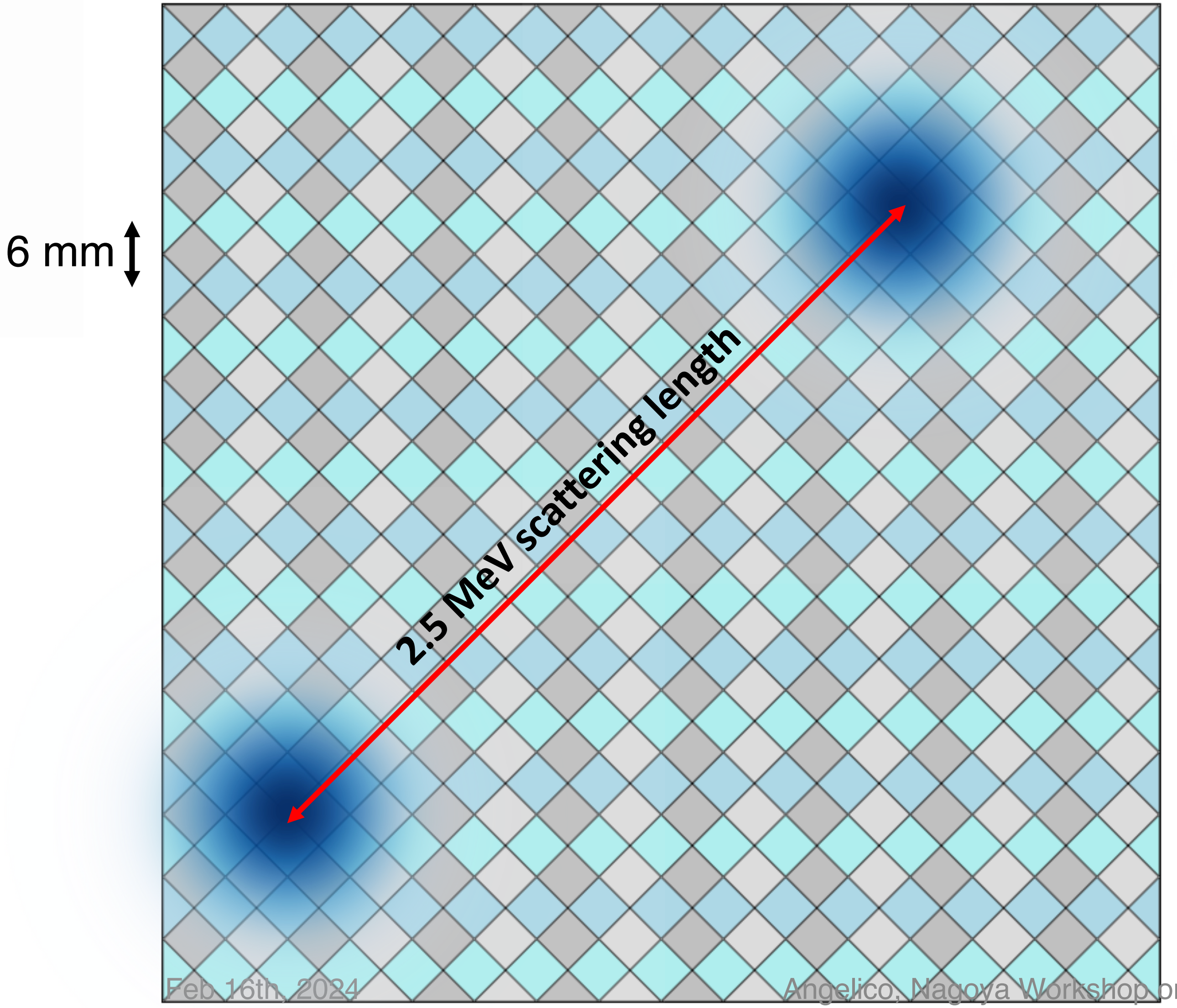
A 6 mm pitch of electrodes balances:

- Ability to separately identify multiple charge depositions (**multi-site** background discrimination)
- **Position resolution** of ~1 mm using sharing of charge across multiple channels
- **Capacitance** scales with the geometry of the electrodes: too large will degrade charge-energy resolution

Li, Z et al. "Simulation of Charge Readout with Segmented Tiles in nEXO." Journal of Instrumentation 14, no. 09 (September 2019): P09020. https://doi.org/10.1088/1748-0221/14/09/P09020.

Charge tile design and fabrication

showing the effect of transverse diffusion



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Amplifying and digitizing in the liquid

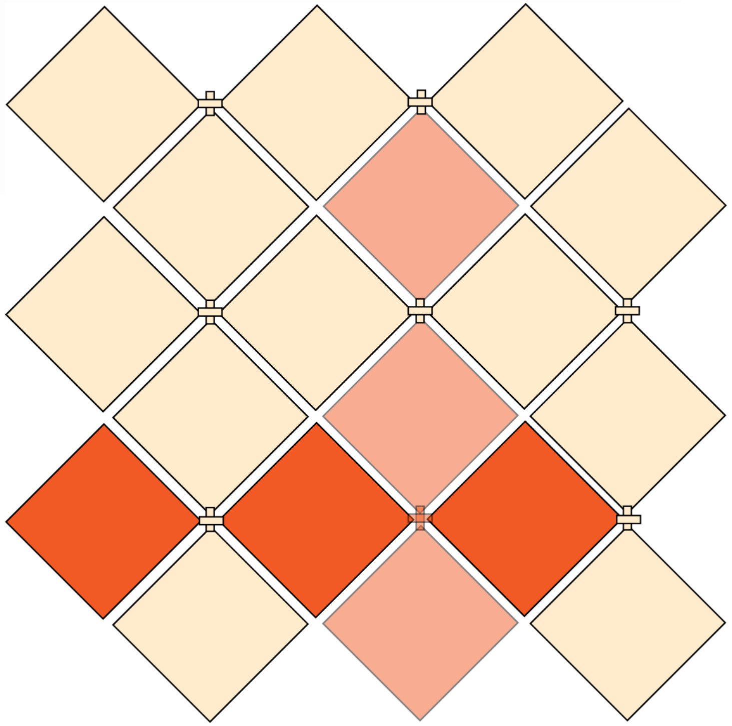
Reduces electrical noise due to unintended capacitances

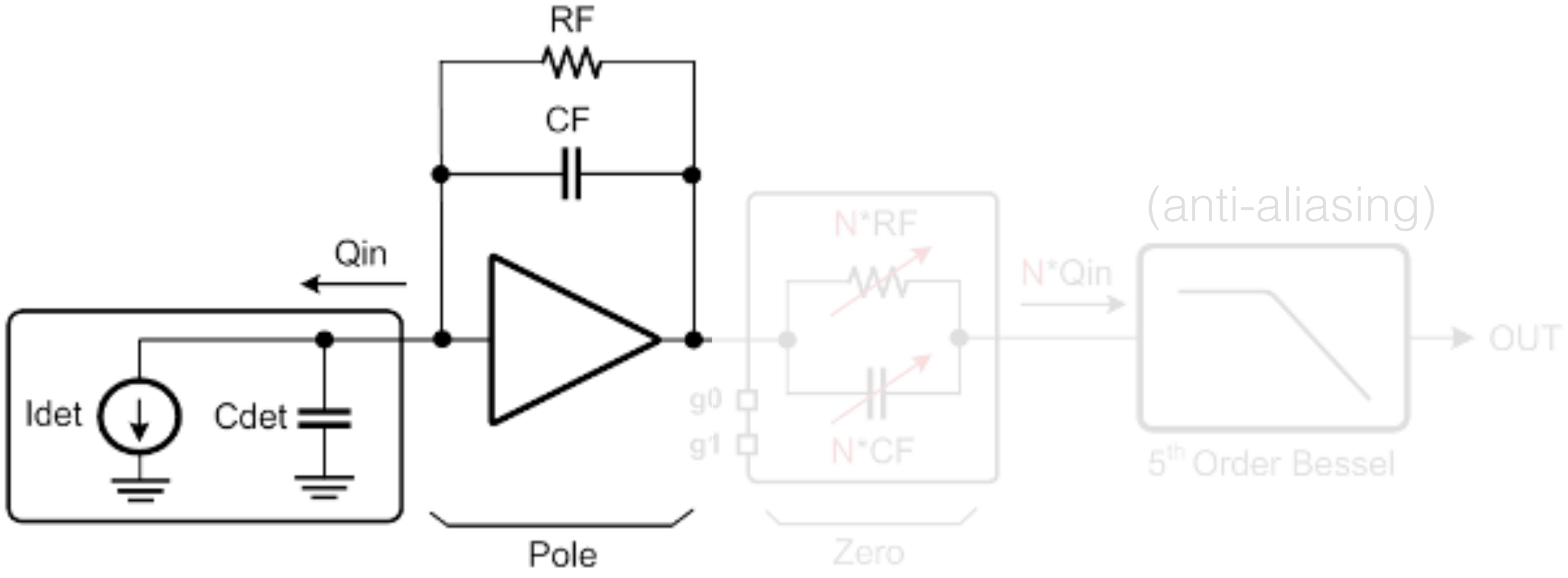
Reduces the quantity of radioactive materials

Retains the fidelity of high frequency electrical signals

An example of a charge detection circuit

$$Q = CV$$

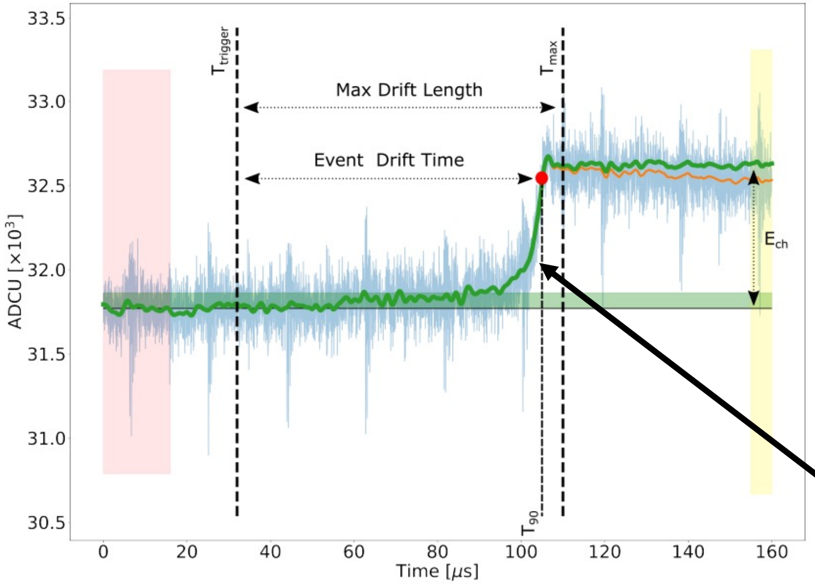




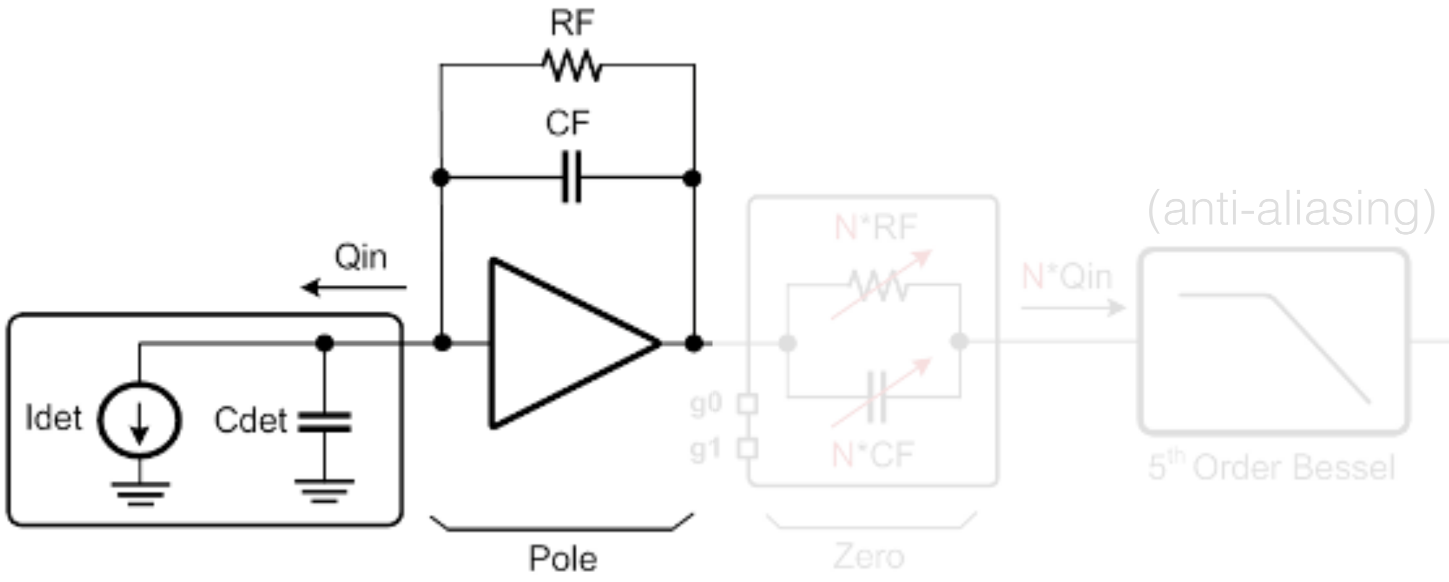
capacitance contributes to stochastic noise

An example of a charge detection circuit

$$Q = CV$$



Dalmasson, Jacopo; 2023. Large detectors for rare event searches. https://purl.stanford.edu/gm128mr9901

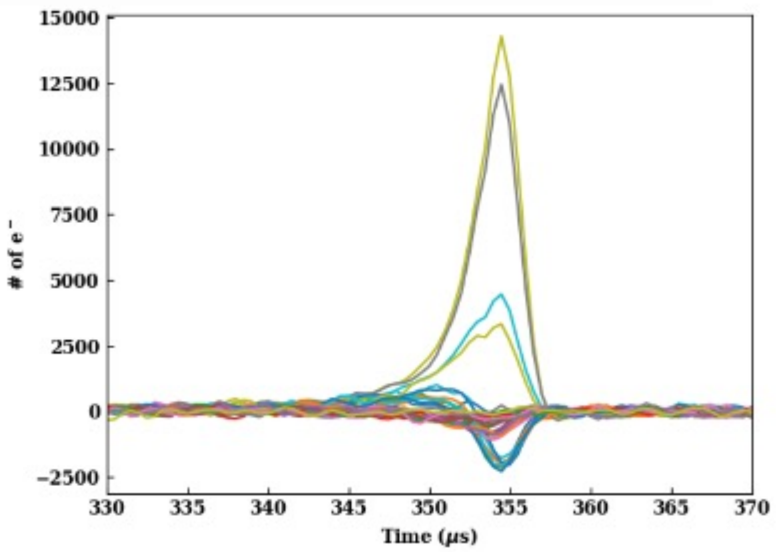


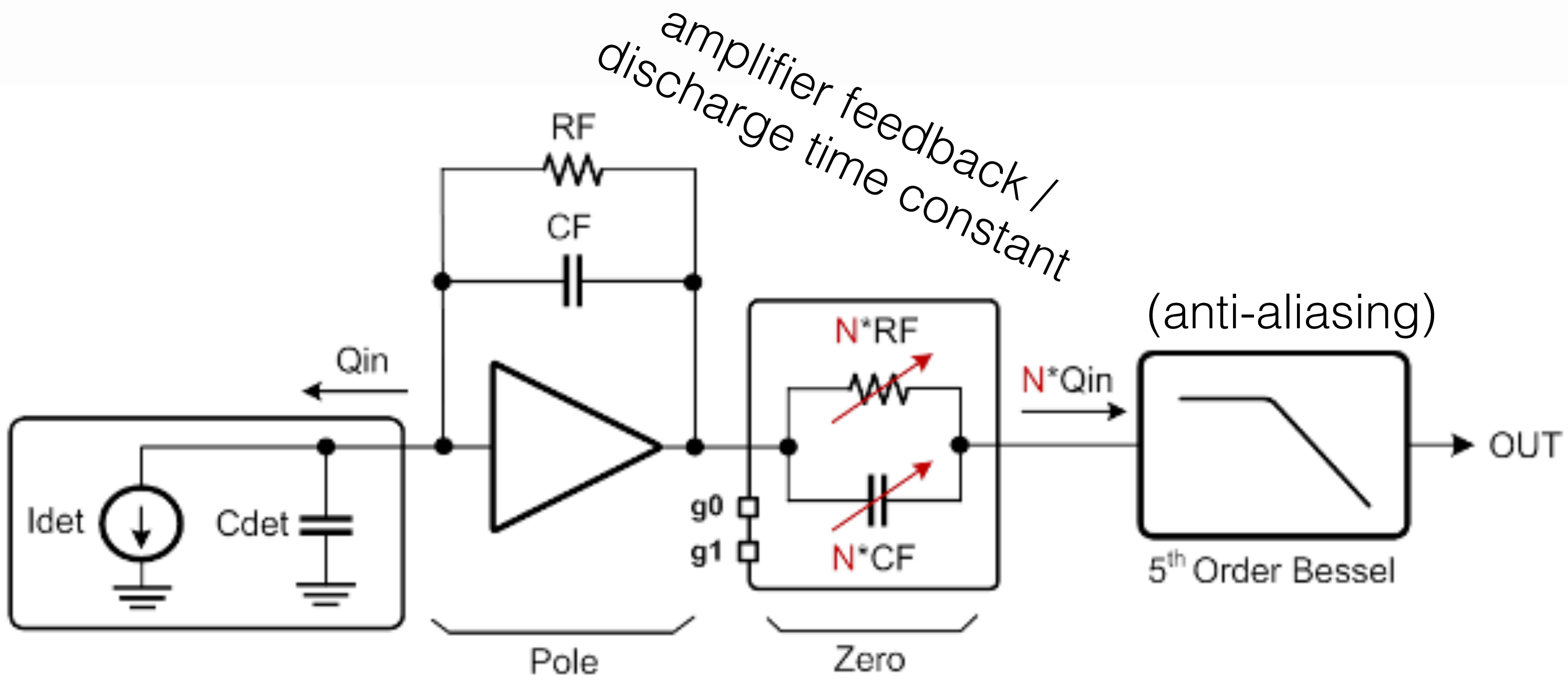
rising edge is charge cloud drifting closer and closer to electrode, inducing charge

An example of a charge detection circuit

nEXO

$$Q = CV$$





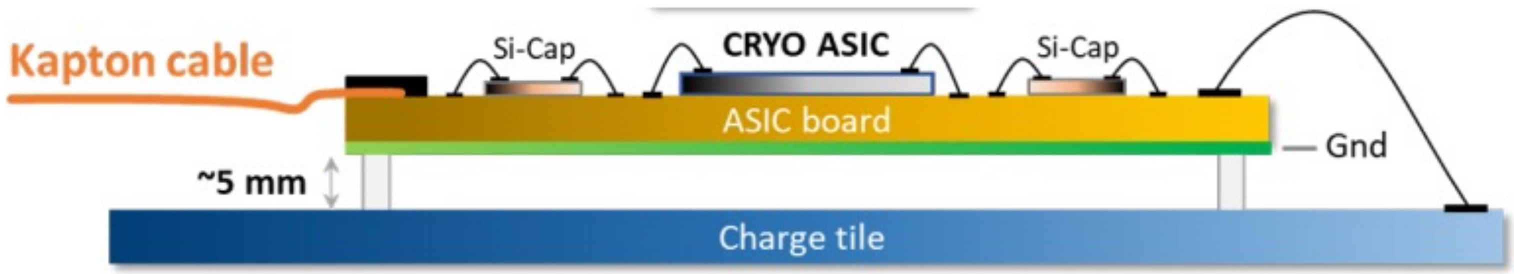
(happens to be the diagrammatic front-end of the ASIC described shortly)

Amplification and digitization electronics

Charge integrating analog circuits have noise contributors often dominated by **capacitance** of the collecting electrode

→ Long cabling introduces a lot of capacitance

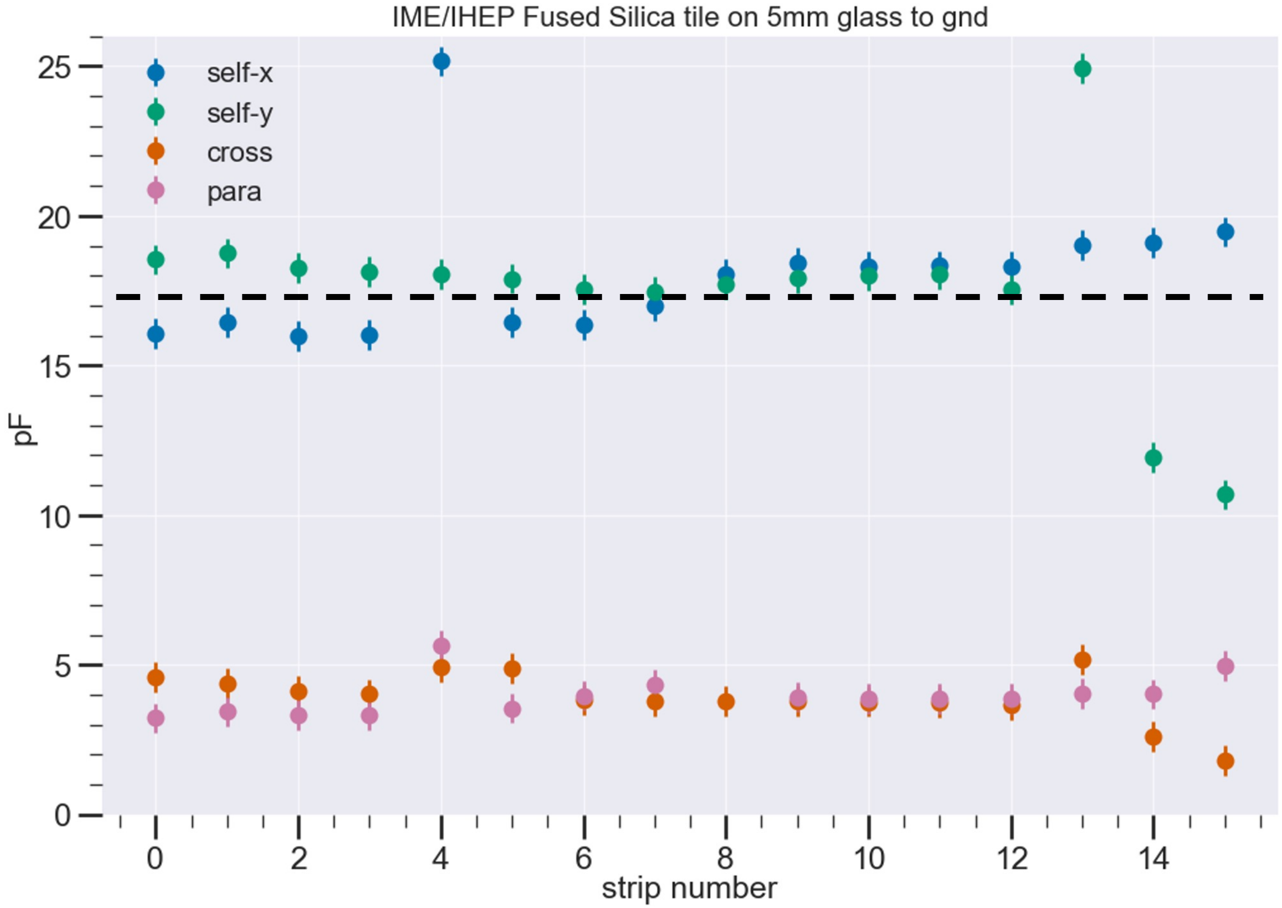
→ Place the amplifier/digitizer as close to the electrode as possible



Place an amplifier AND digitizer directly on the back of the modular charge tiles

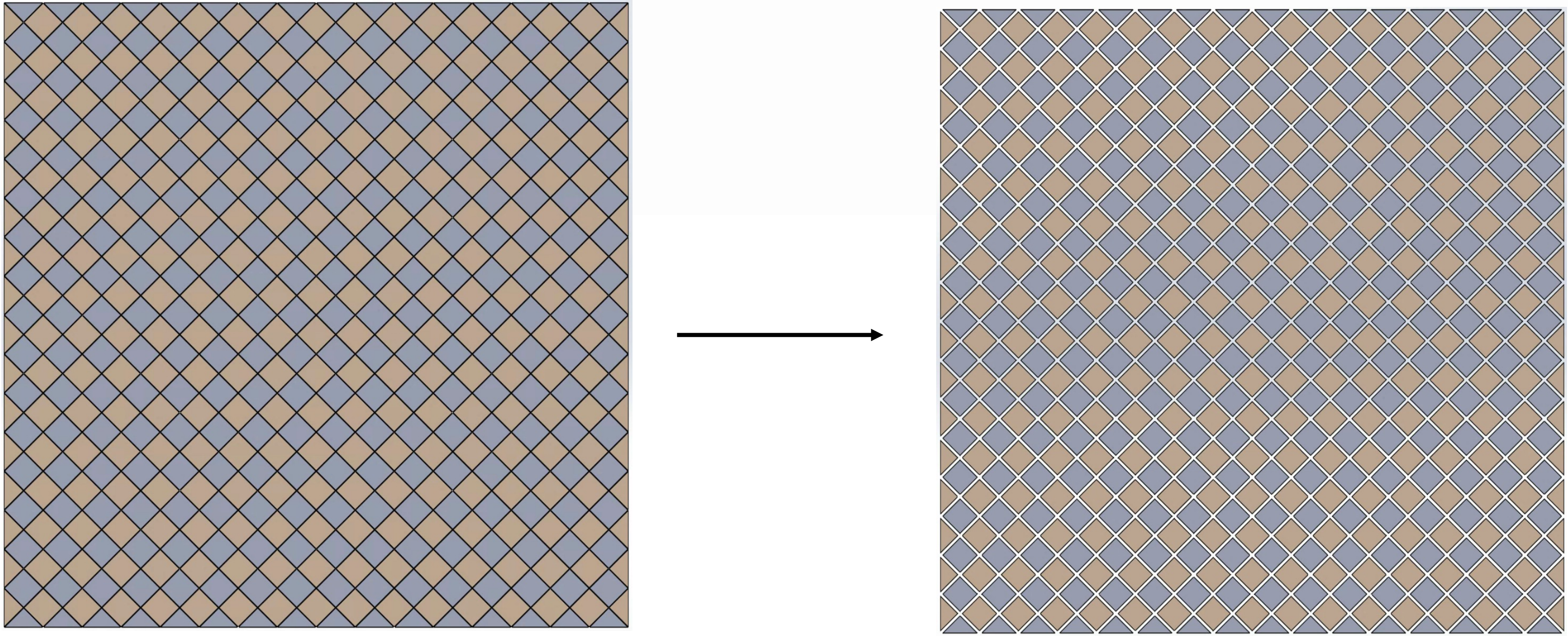
Capacitance of tiles

Prototype from IME/IHEP discovered shipping risks

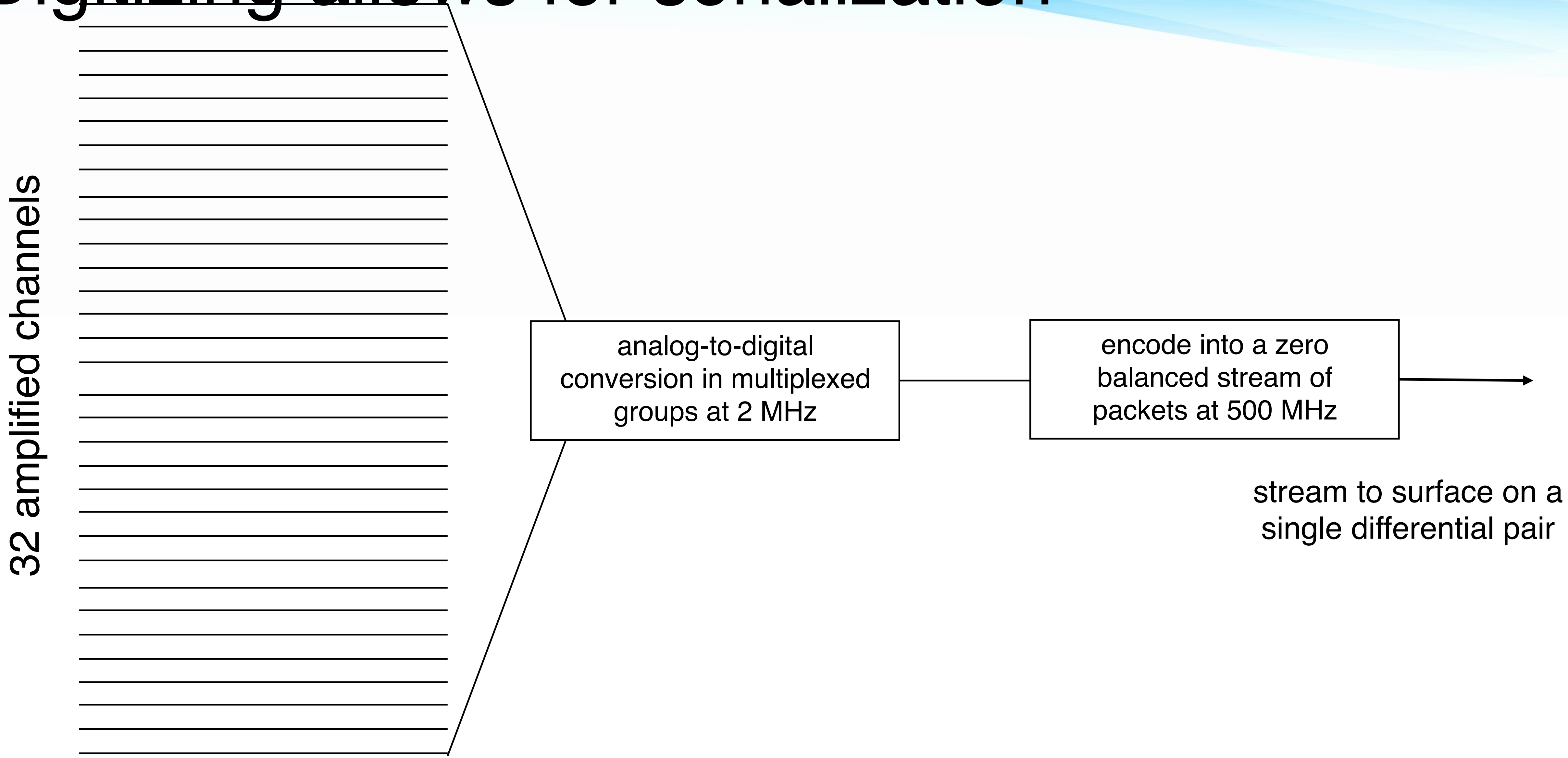


Capacitance of tiles

Tile design involves looking at ways to reduce the capacitance



Digitizing allows for serialization



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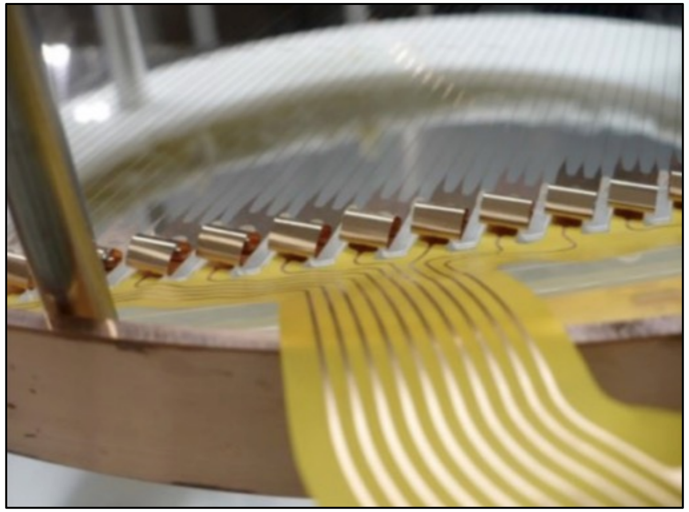
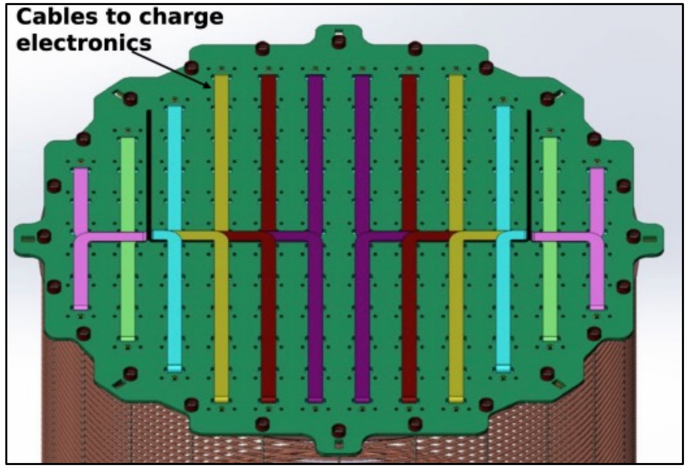
nEXO has strict **radiopurity** requirements and assays every material that goes into the detector

→ ~3840 channels implies lots of cable mass if every channel gets a cable up to the surface

EXO-200 analog charge-readout cabling





nEXO conceptual layout of flexible cabling above anode

Amplification and digitization electronics

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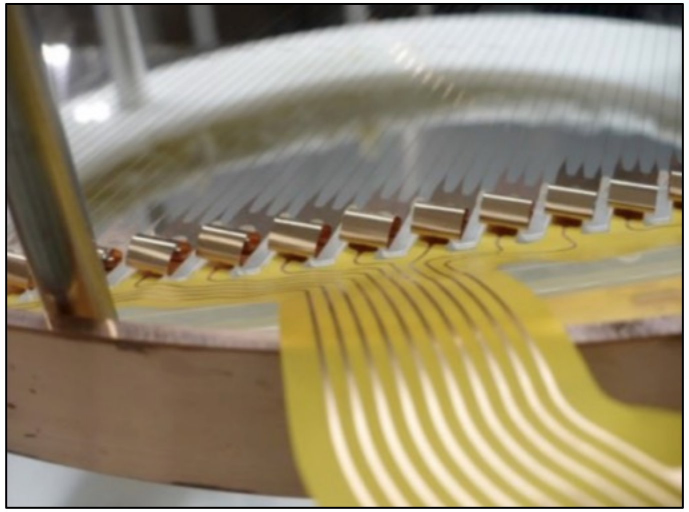
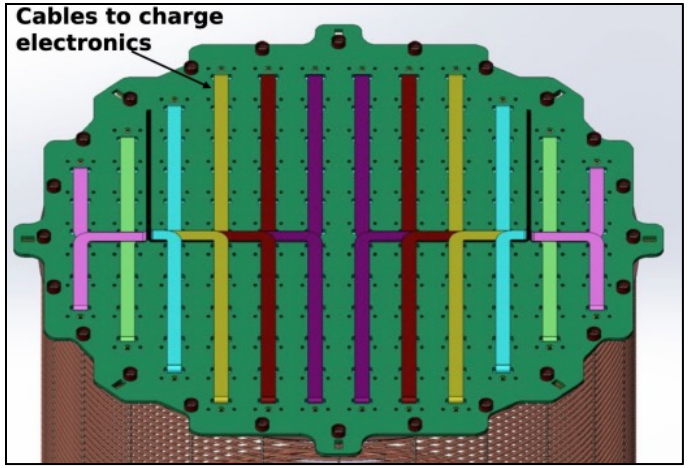
Typical lines going to and from an ASIC: power, data, slow controls

Can group and bus power and slow controls, reducing even further the number of lines (but balancing risk of possibly losing a group)

EXO-200 analog charge-readout cabling



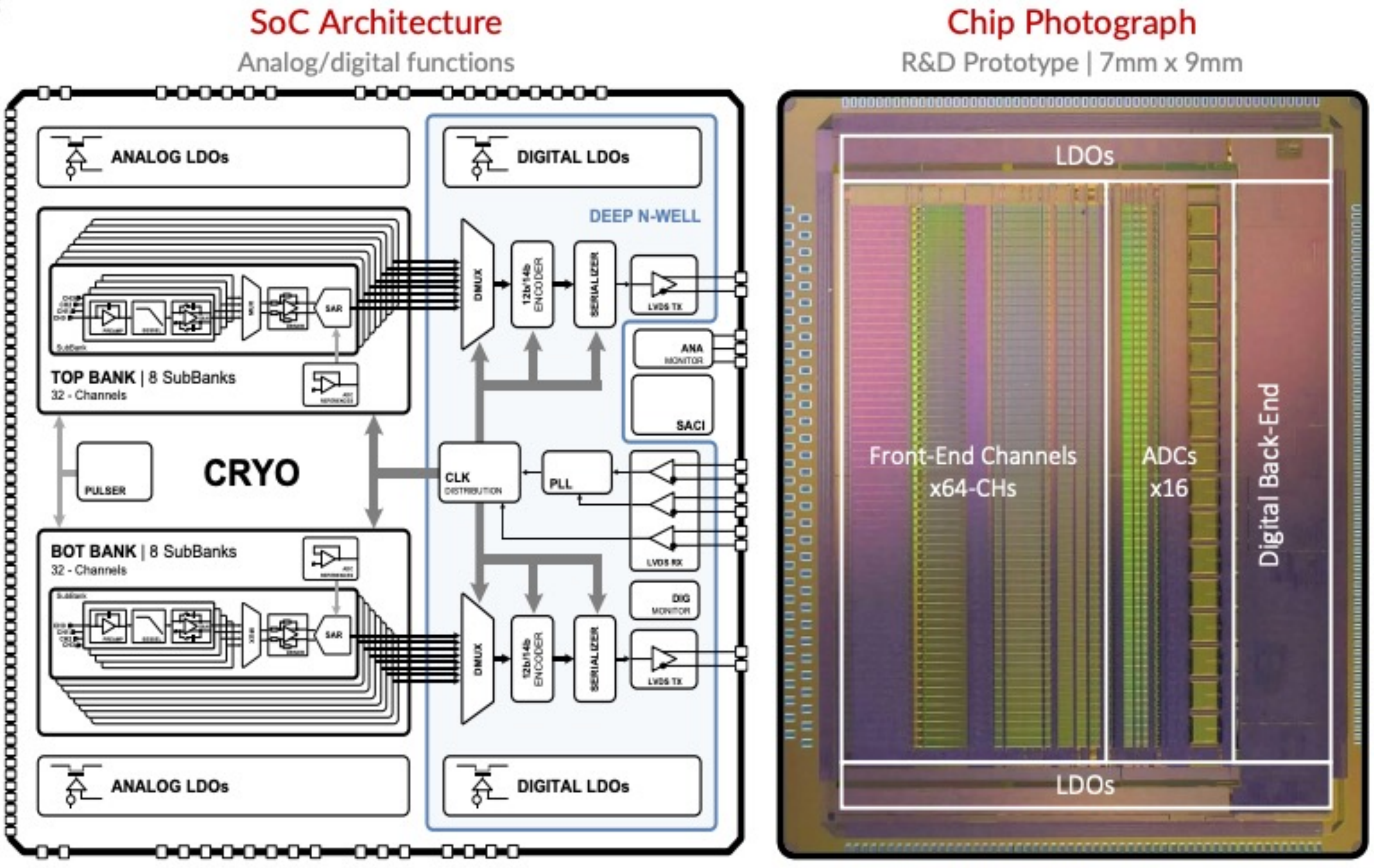


nEXO conceptual layout of flexible cabling above anode

System on chip, CRYO ASIC, from SLAC TID-AIR

CRYO ASIC – R&D prototype

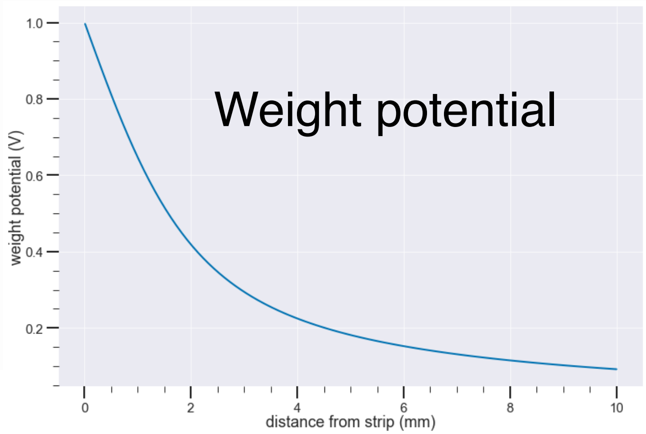
Aldo Pena-Perez, Dionisio Doering, Aseem Gupta, Camillo Tamma, Bojan Markovic, Hussein Ali, Pietro Caragiulo, Lorenzo Rota, Umanath Kamath, Savino Petrignani, Xiaobin Xu, Faisal Abu-Nimeh, P. A. (Sander) Breur, Patrick Tsang, Mark Convery, and Angelo Dragone



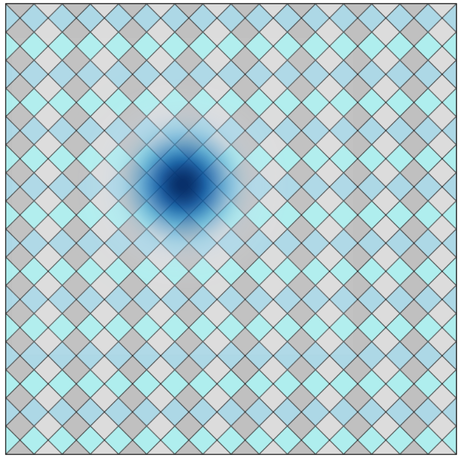
CRYO ASIC Specifications

TPC Experiment	nEXO			
CMOS process	130nm			
Supply voltage	2.5V (2V, 1V internal)			
Input capacitance	~ 20pF - 30pF			
Anti-aliasing filter	5^{th} order Bessel architecture			
Peaking times	0.6us, 1.2us, 2.4us, 3.6us			
Gain settings	6.0X (57.2mV/fC)	3.0X (28.6mV/fC)	1.5X (14.3mV/fC)	1.0X (9.6mV/fC)
Max. input charge	25fC	50fC	100fC	150fC
Noise	< 150e- @ 3.0X and 1.2us			
ADC	12-bit 2MSPS / CH			
INL and DNL	±1LSB			
Power Consumption	< 15mW / CH (32-CH version)			
Temperature	LXe ~165K (-113°C)			

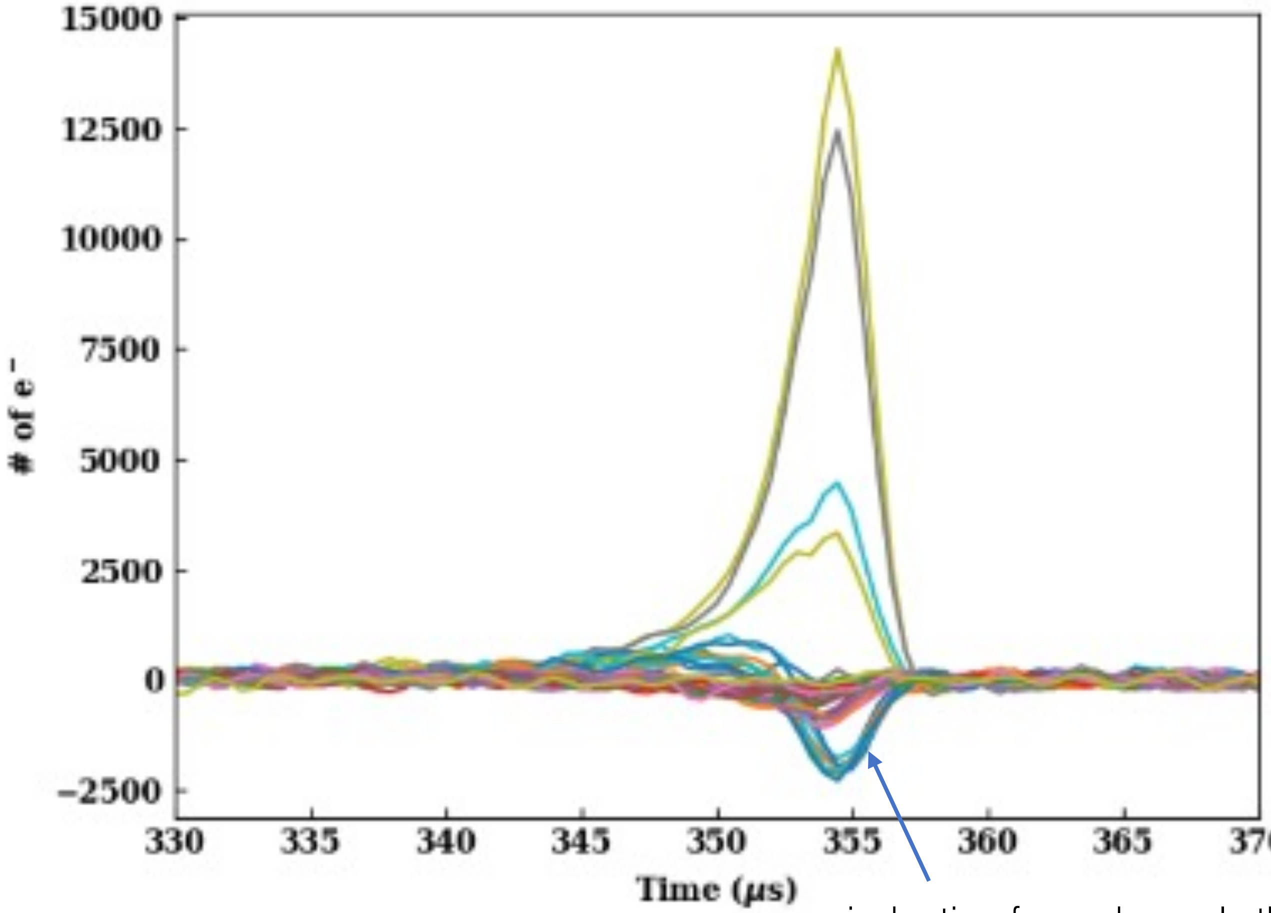
Impulse response convolved with simulated drifting electrons



+

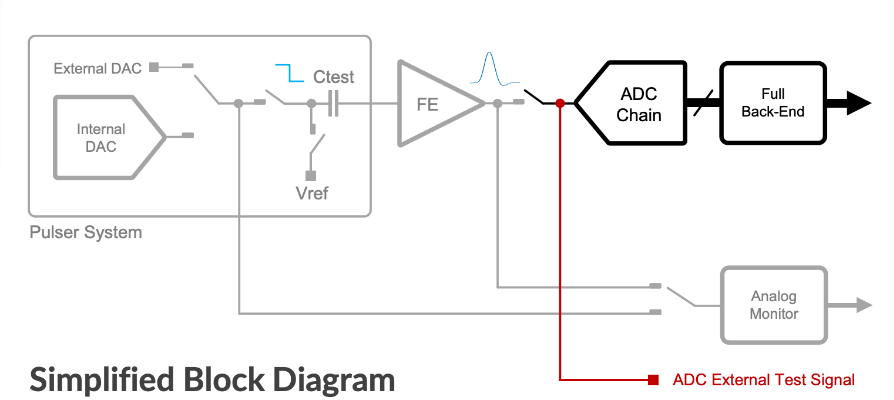


nEXO charge waveform level simulation interfacing with G4

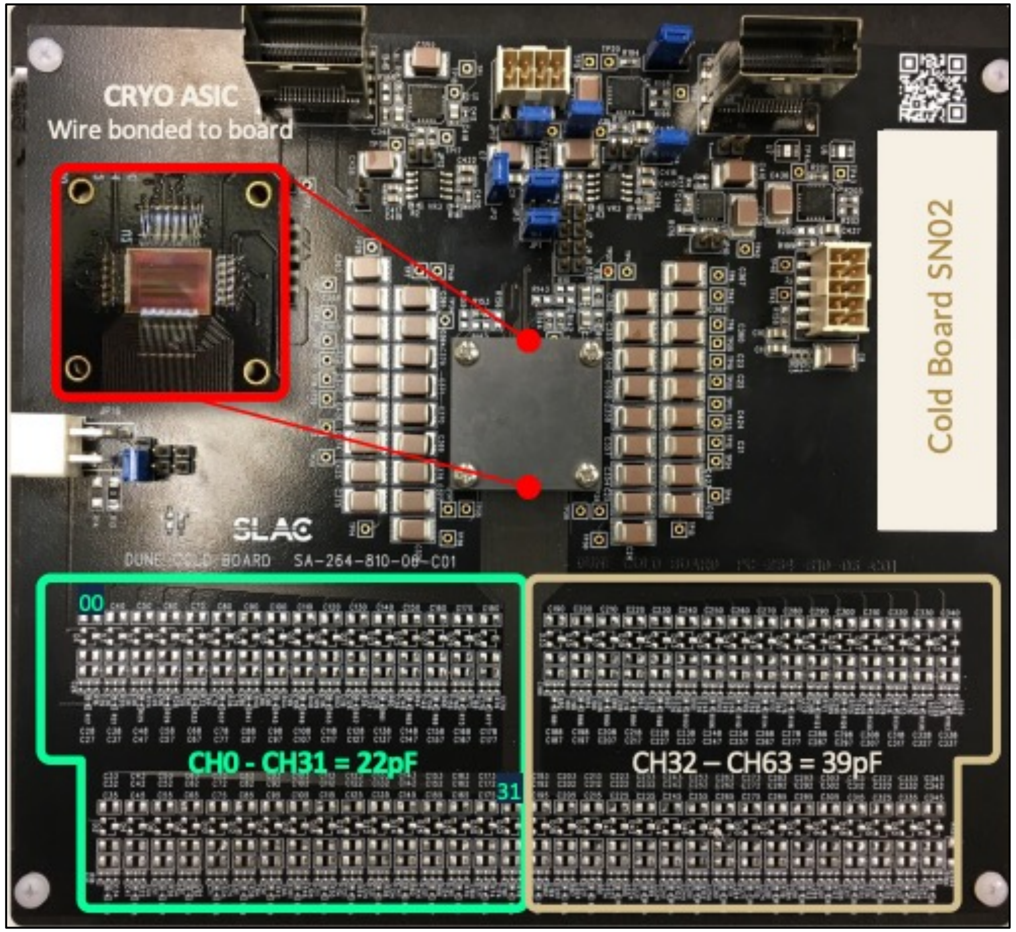


induction from channels that do not collect charge

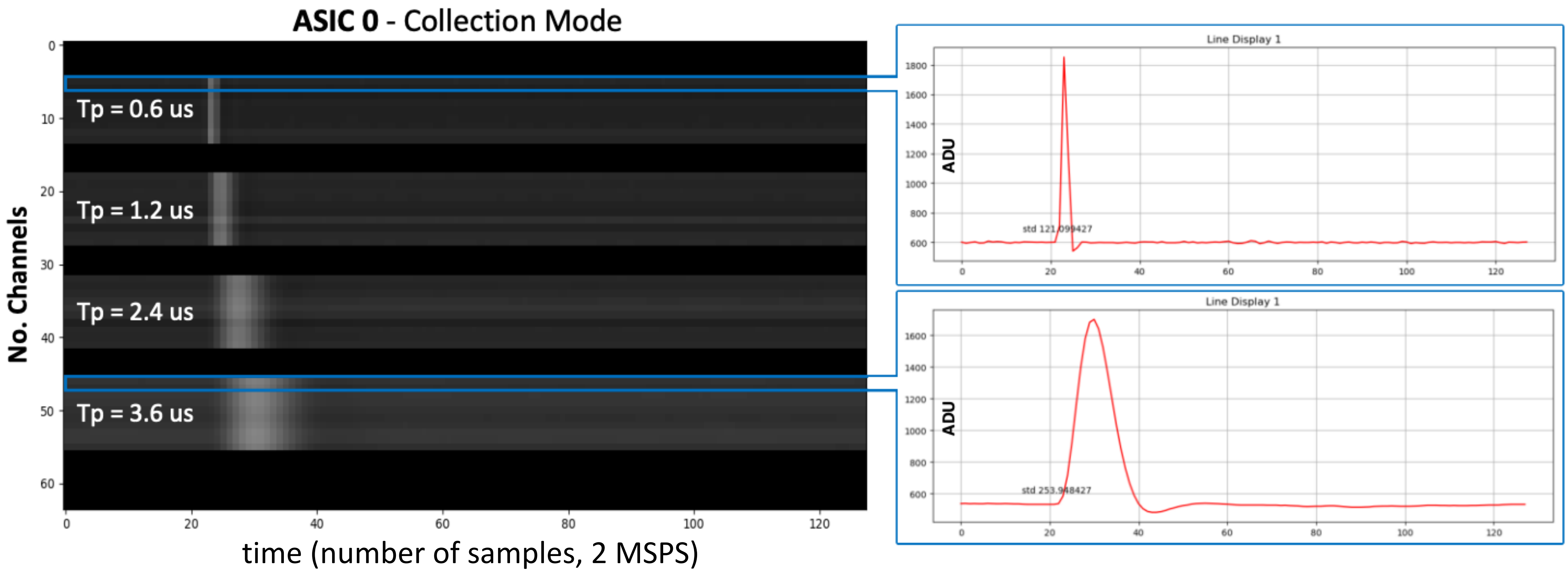
Bench-top and cold tests have been numerous using FR-4 ASIC boards



Simplified Block Diagram
CRYO in test mode (ADC section)



Bench-top and cold tests have been numerous using FR-4 ASIC boards



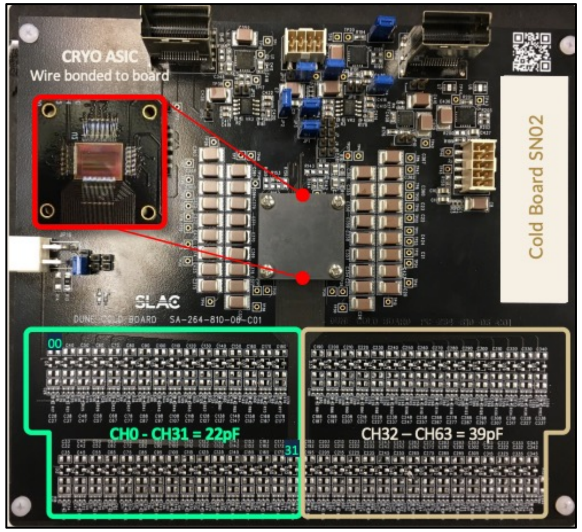
Screenshots from “live” oscilloscope view software: firmware and control software is well developed

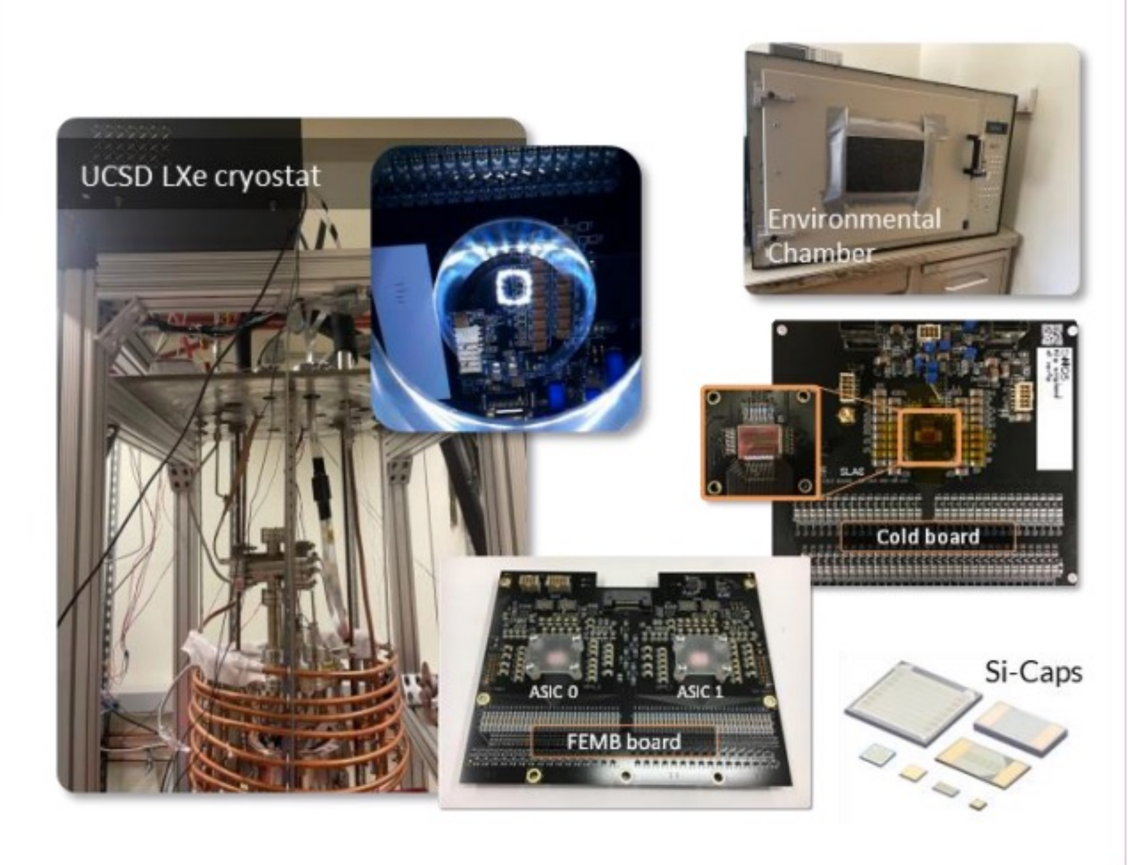
Noise measurements at UCSD

University of California, San Diego (UCSD)
Prof. Liang Yang with Zepeng Li and students

Has a LXe cryostat and test-boards that can attach lumped element capacitances to the inputs of the ASIC for bench-top and cold performance testing

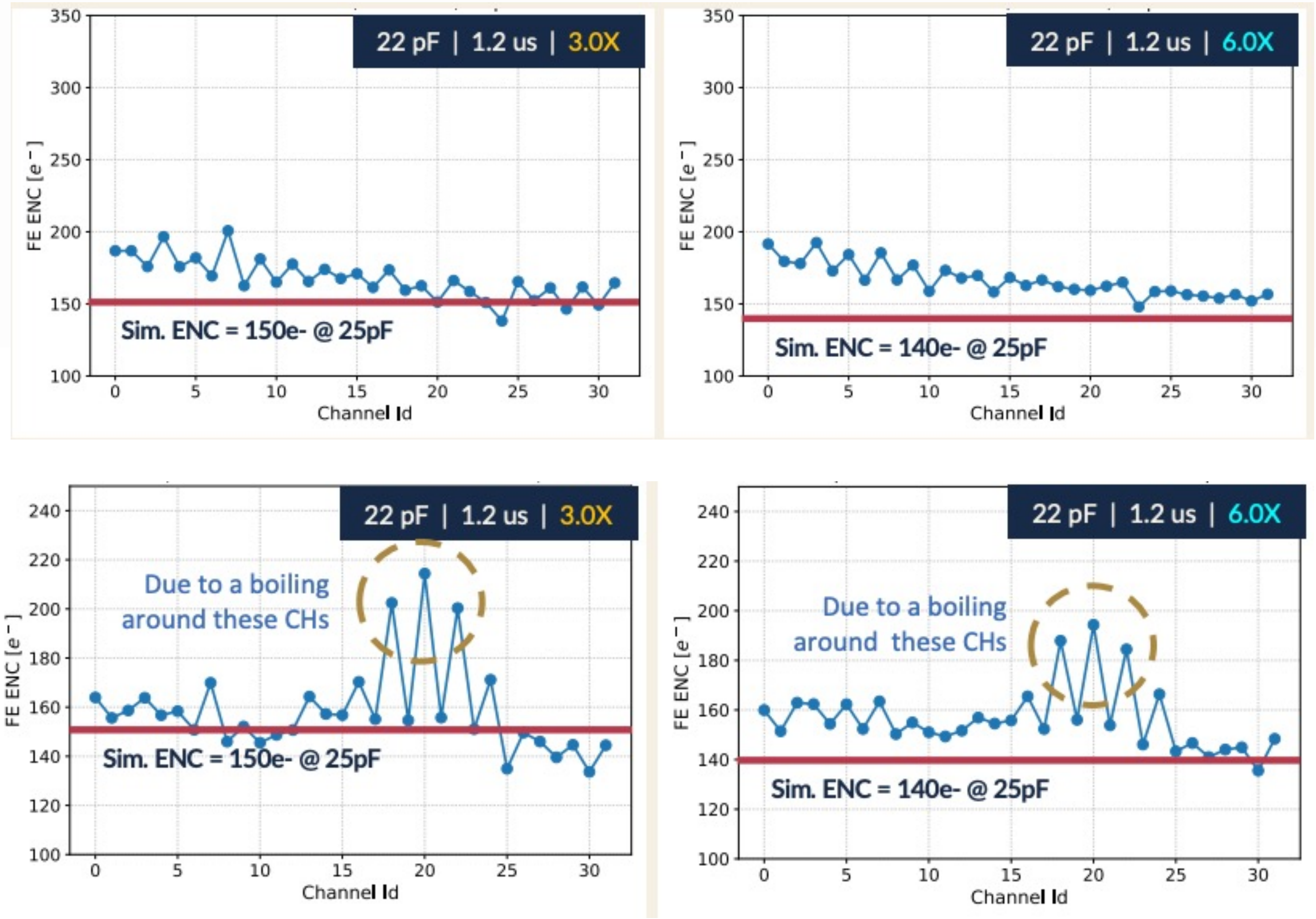
A camera is installed that can observe boiling under much lower pressure conditions than nEXO from power dissipated in the ASIC





Noise measurements at UCSD

Lower gain mode | nEXO nominal gain mode



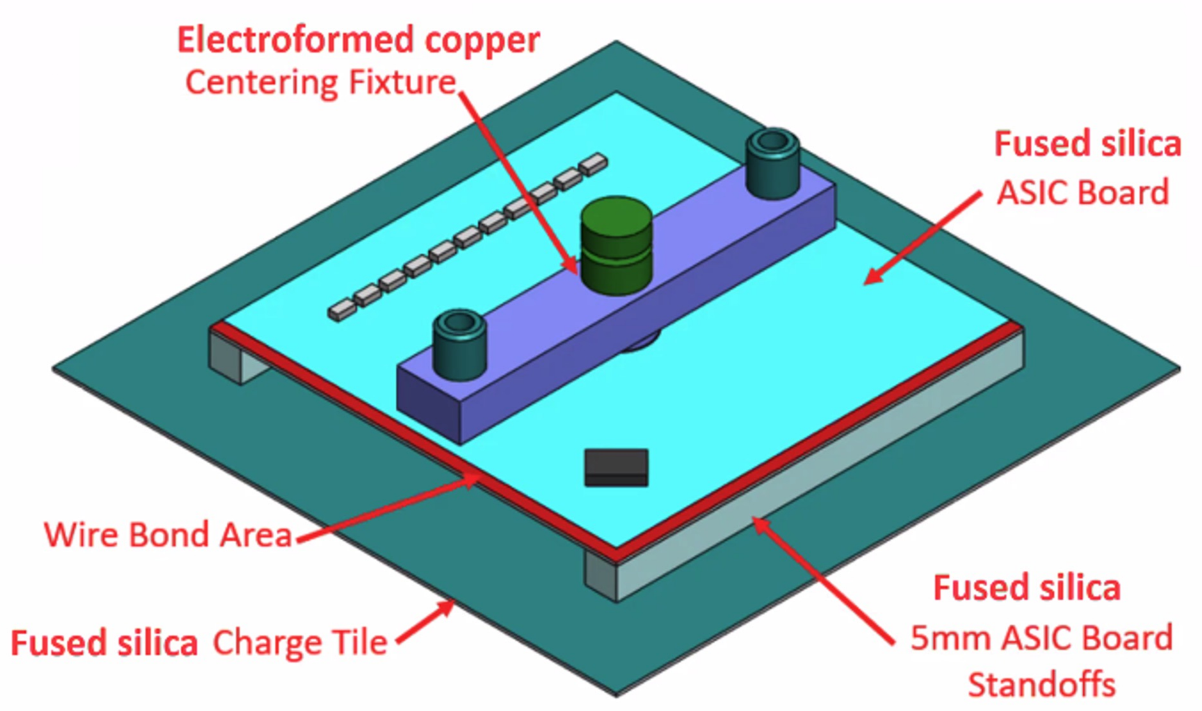
In gas at 170K

Matching expectation, within knowledge of stray capacitances

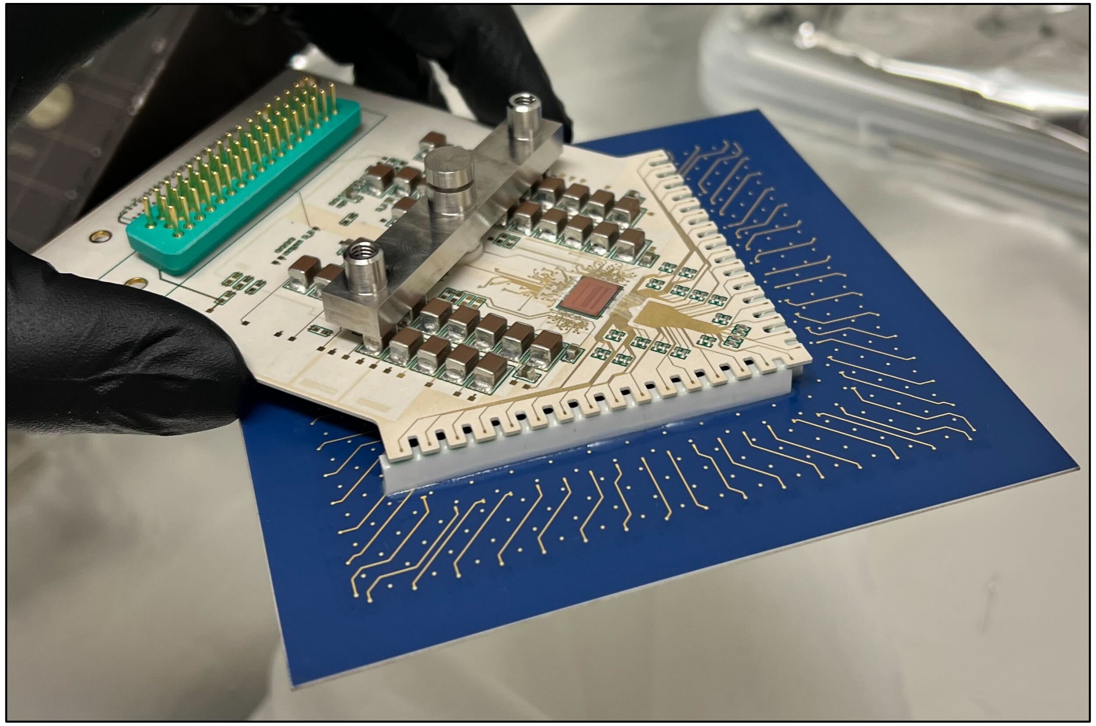
In liquid at 170K

at somewhat low pressure. Boiling has been shown to go away with moderate increase in pressure (>1.05 bar)

What do we learn by integrating electronics with prototype tiles, nEXO vs lab-scale

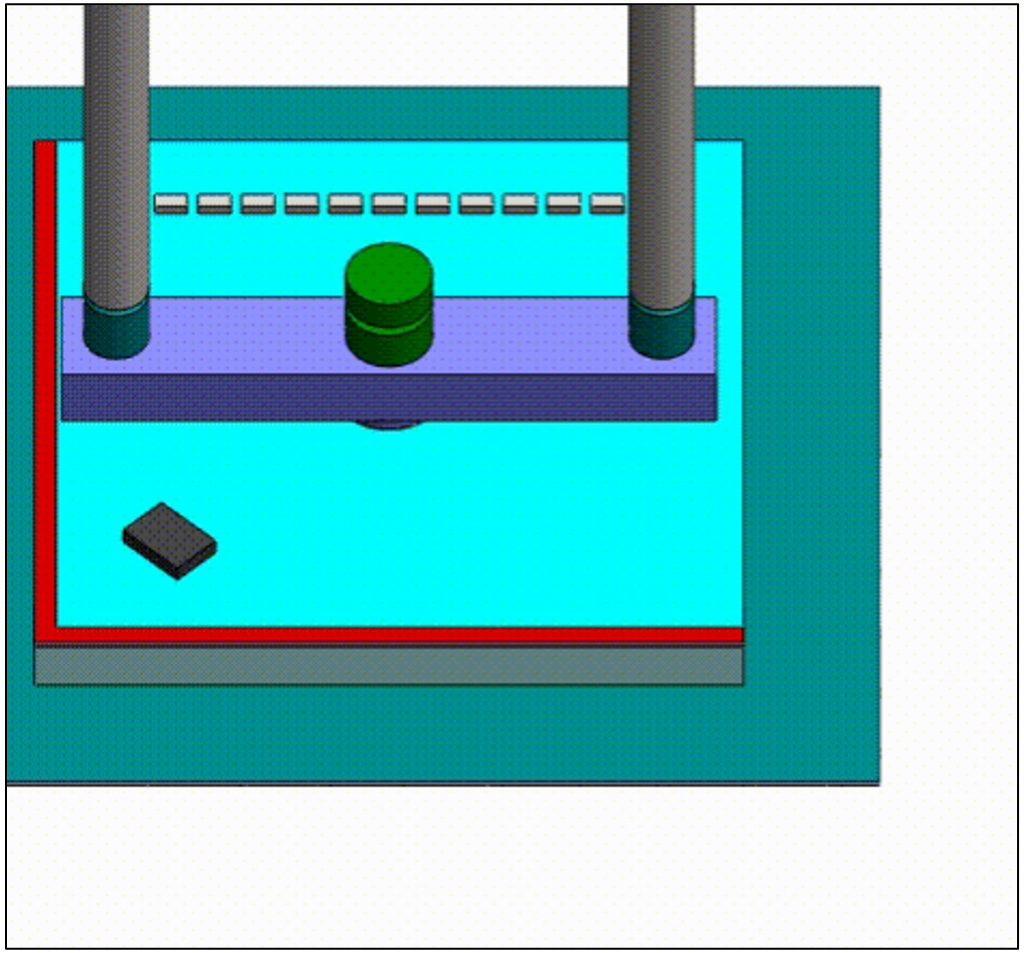


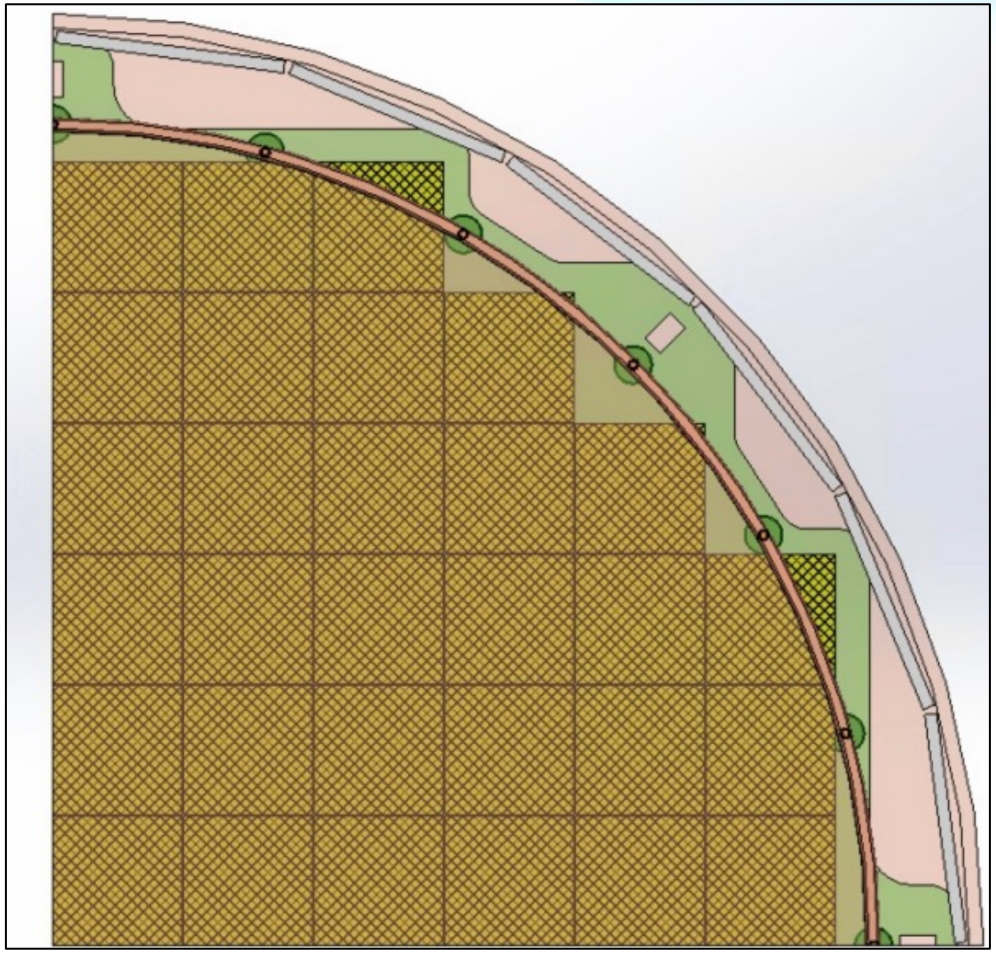
nEXO concept: radiopure materials stacked together with epoxy



Prototype module at Stanford lab: not radiopure, but electronegative pure

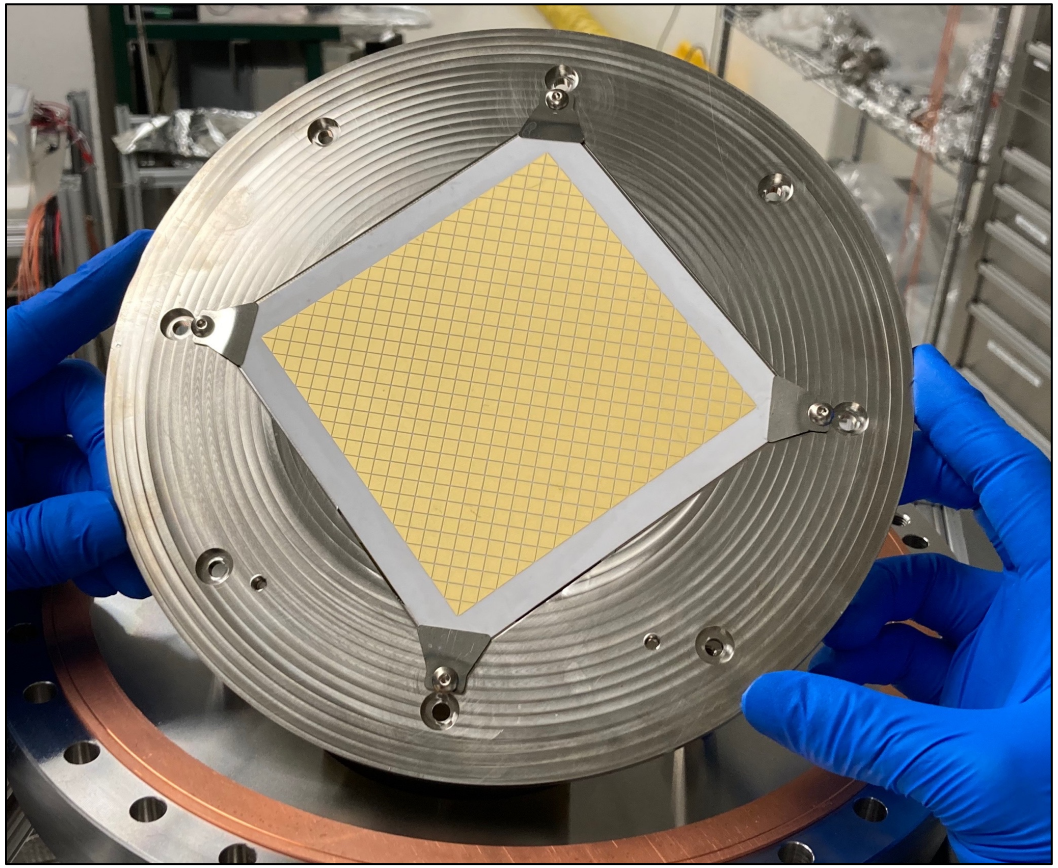
nEXO charge-tile array engineering





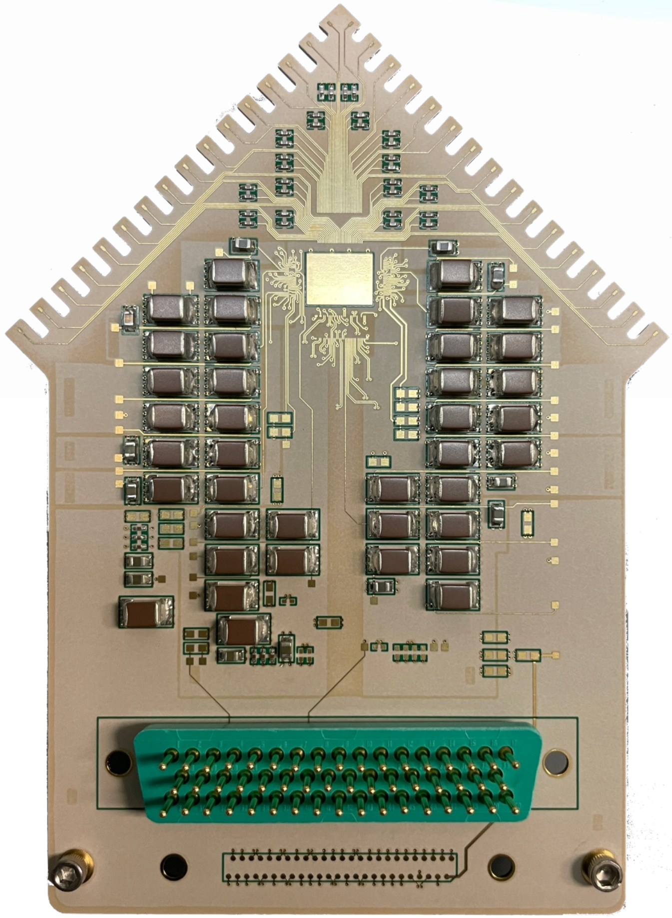
Engineers and scientists at Pacific Northwest National Laboratory (PNNL) working on mechanical holding, tolerance for gaps, interfacing with high voltage field cage, …

Test assembly on durable, commercially producible prototypes



"Mock-tile"

Ceramic 4-layer printed circuit board

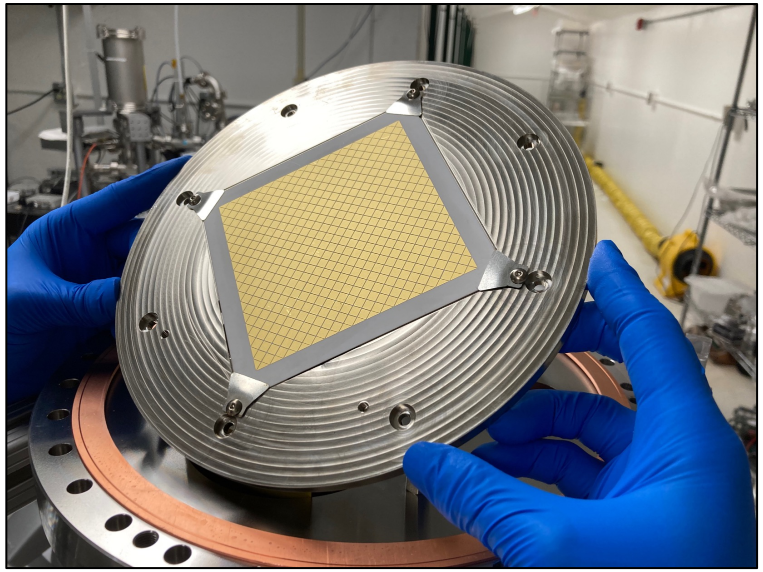


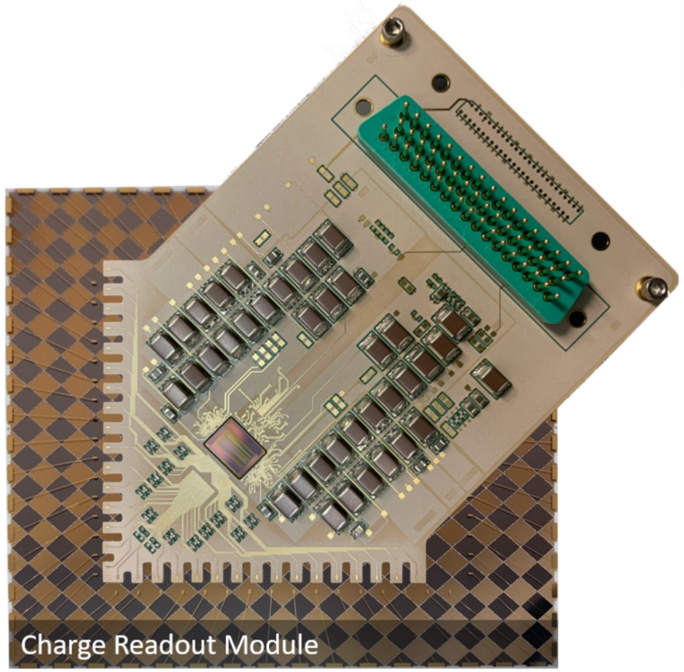
"ASIC Board"

8-layer PTFE-ceramic printed circuit board

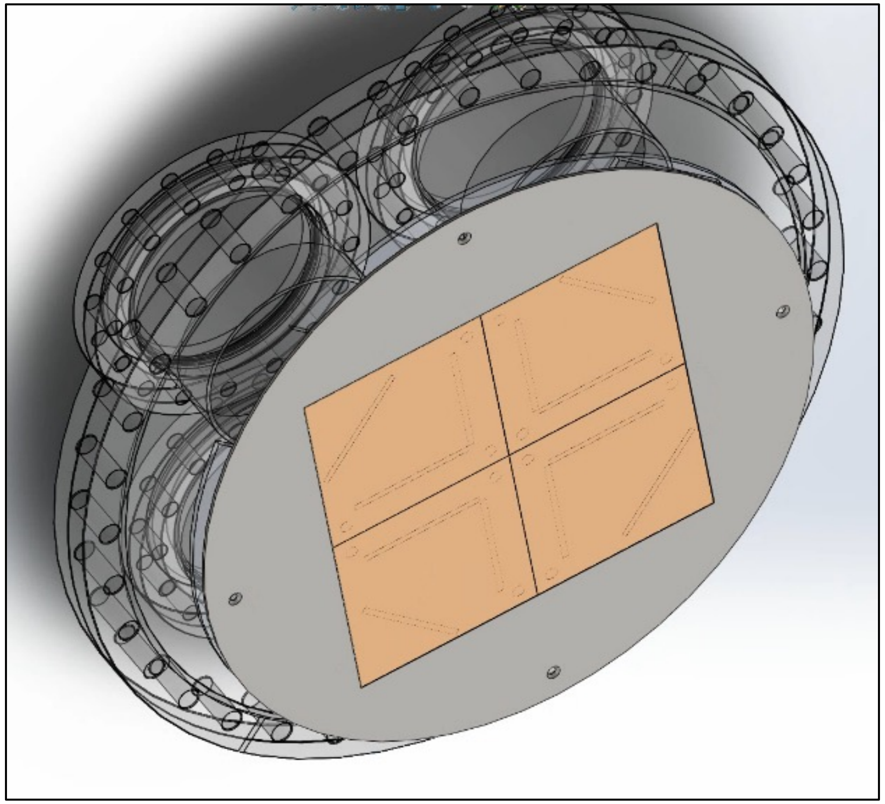
The next year in view

Demonstrate operation of mock-tile modules in liquid xenon → Repeat with a prototype fused silica tile → Scale up in number of modules, and install into a 2x2 array TPC





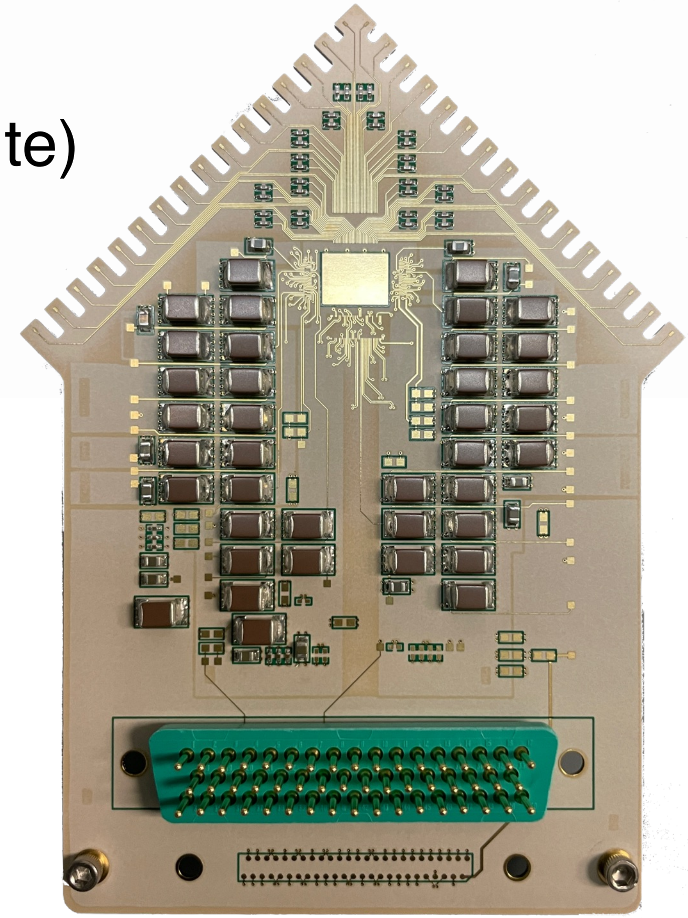
composite image, for now

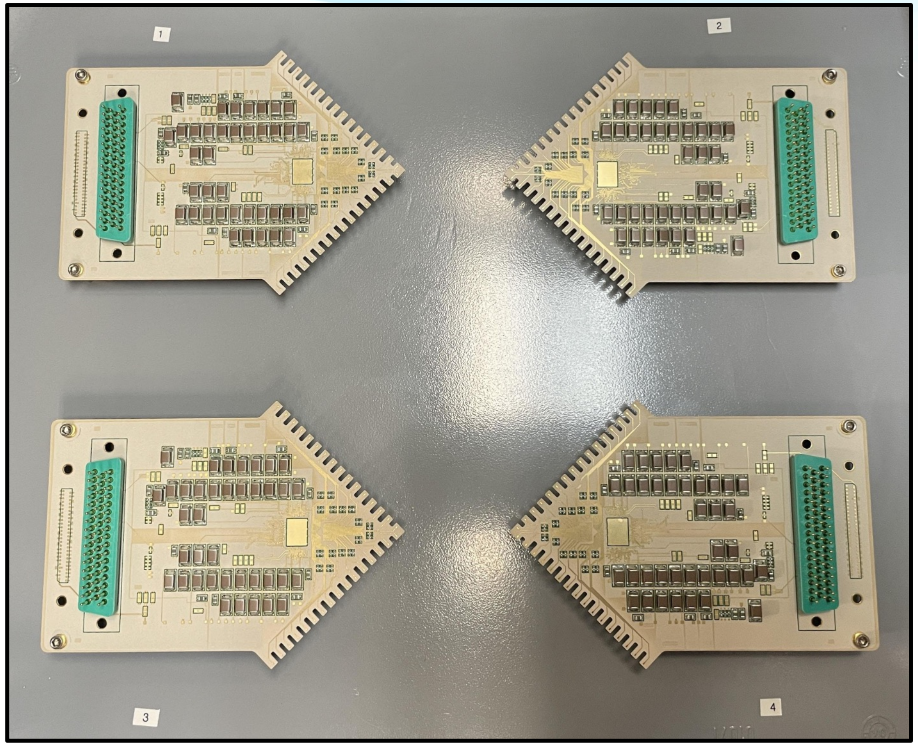


Prototype ASIC Board

8-layer Rogers 3003
(ceramic filled PTFE composite)

- Vacuum compatible capacitors soldered with a flux removal cleaning procedure
- No resistors
- Vacuum compatible accuglass sub-d 50 connector (default)
- Solderless fuzz-button compatible connector pad patter (backup)

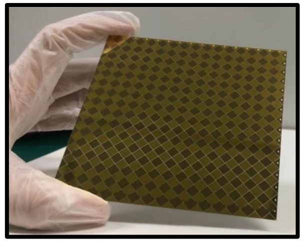




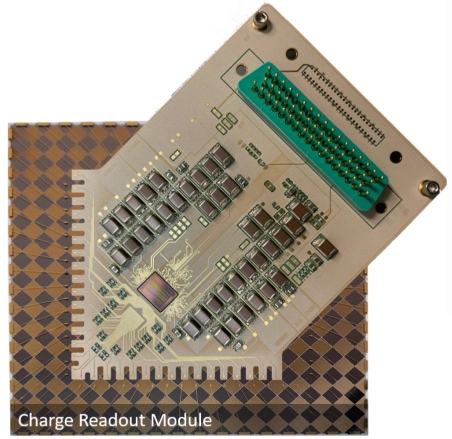
Stages of prototype module assembly

nEXO

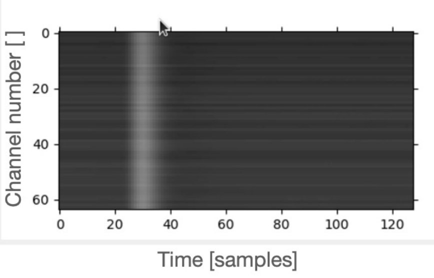
obtain a tile

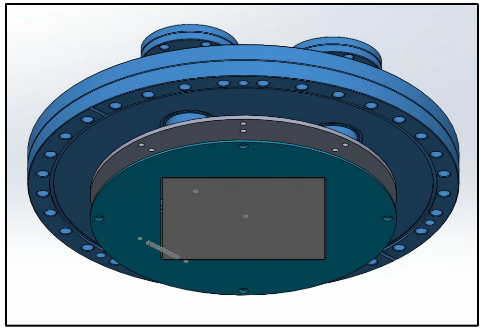


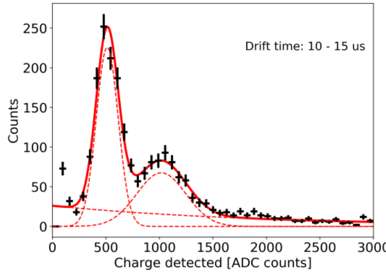
adhere the ASIC board and tile and wirebond



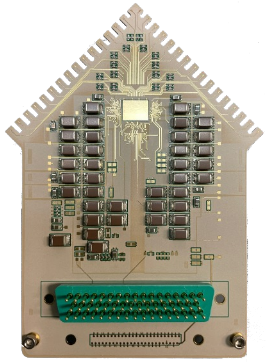
test the ASIC on the bench or in capacitively coupled test stand



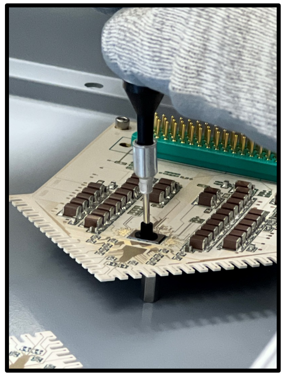




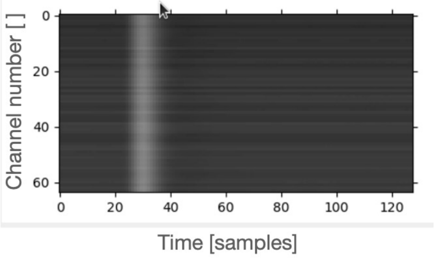
populate ASIC board with components



adhere an ASIC and wirebond



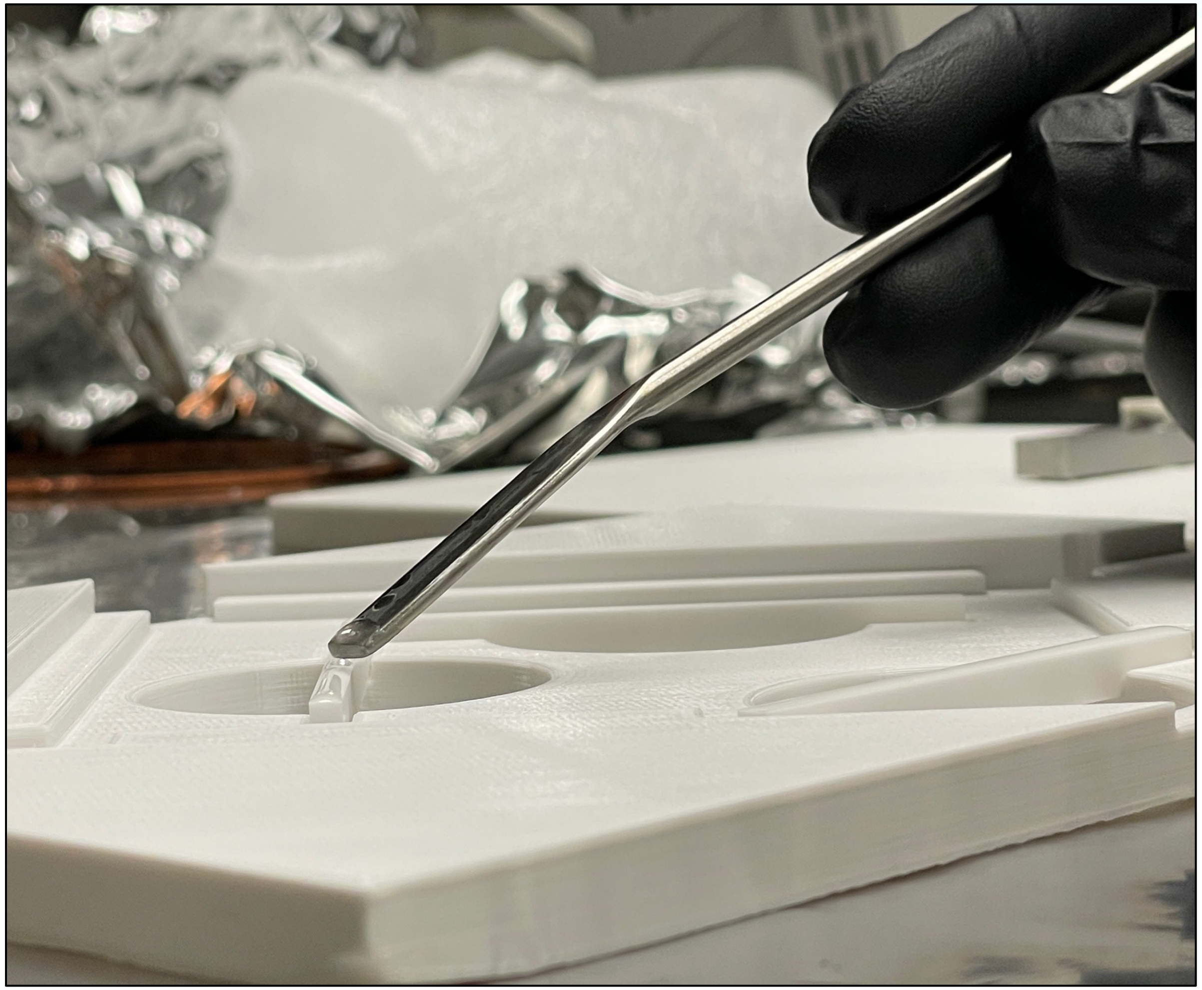
test the ASIC on the bench



Key practical components

Masterbond EP29LPSP

- Two component epoxy with 100:65 ratio, pre-mixed frozen syringes can be bought
- Used in EXO-200 for the feedthrough cabling
  - Relatively far proximity from drift region
- Low outgassing



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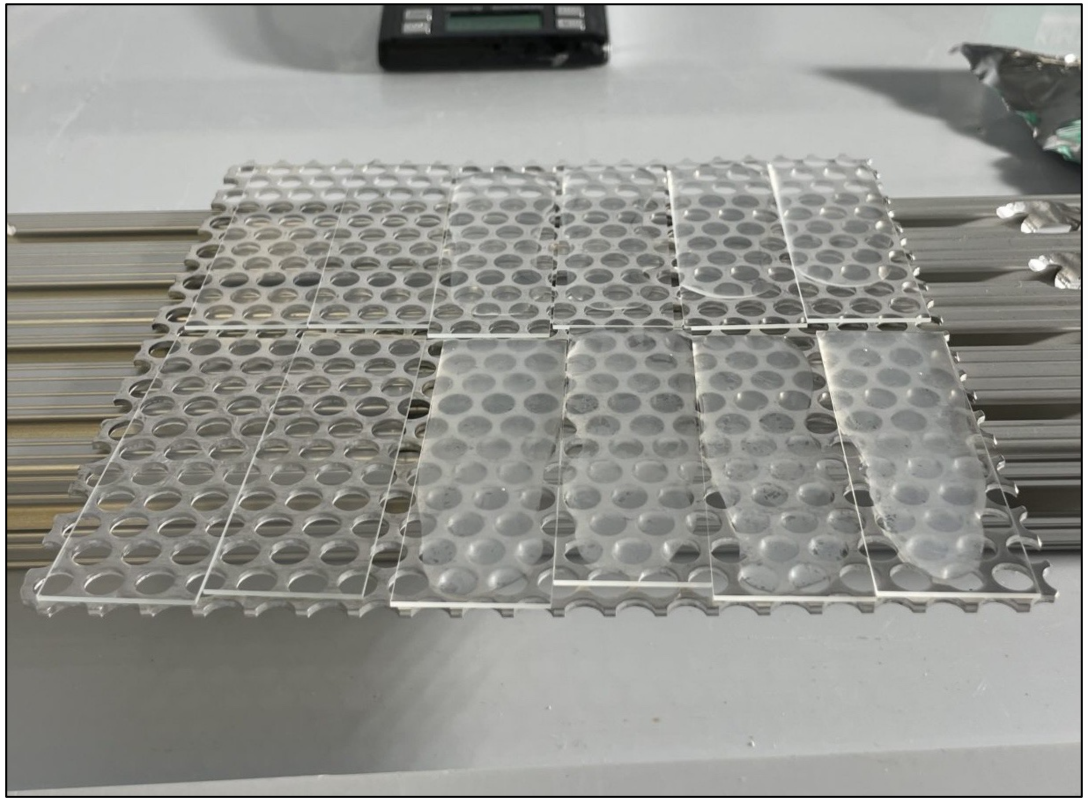
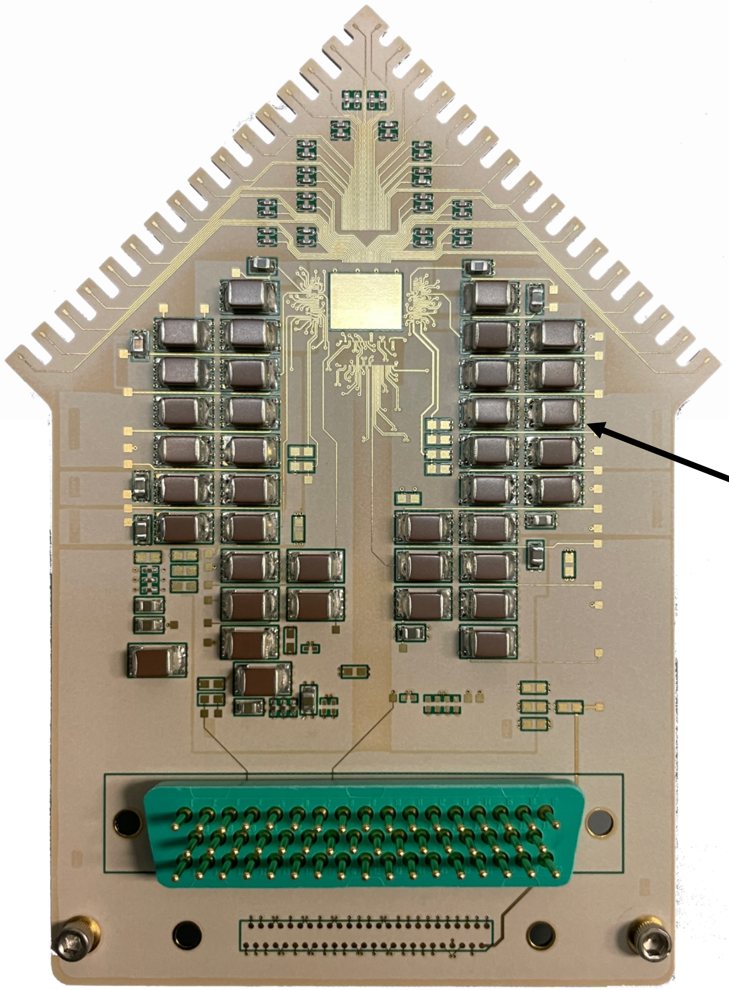


Critical confirmations in progress:

- ~~UHV outgassing measurements~~ (good)
- Liquid xenon electron lifetime measurements
- Radioassay measurements (upper bounds with small masses)

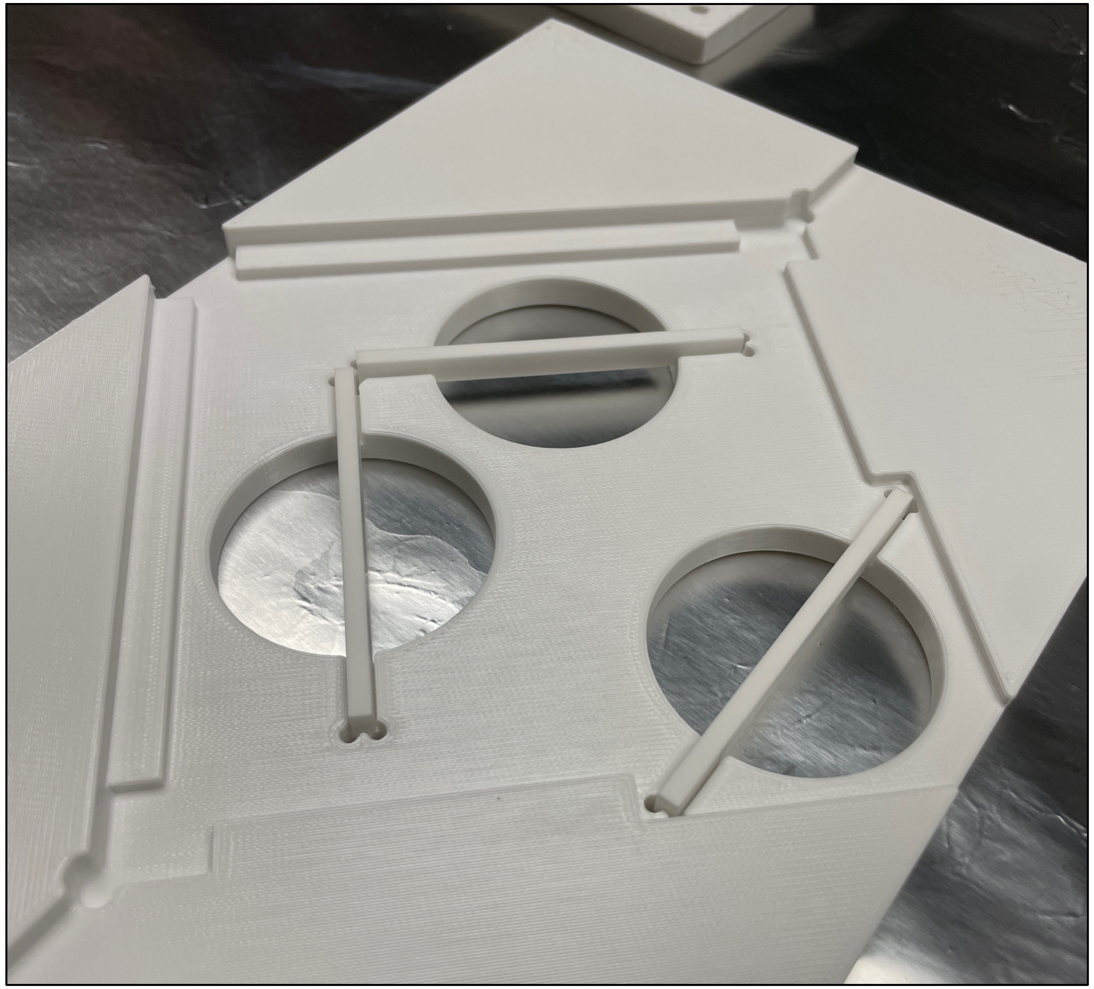
Masterbond in nEXO

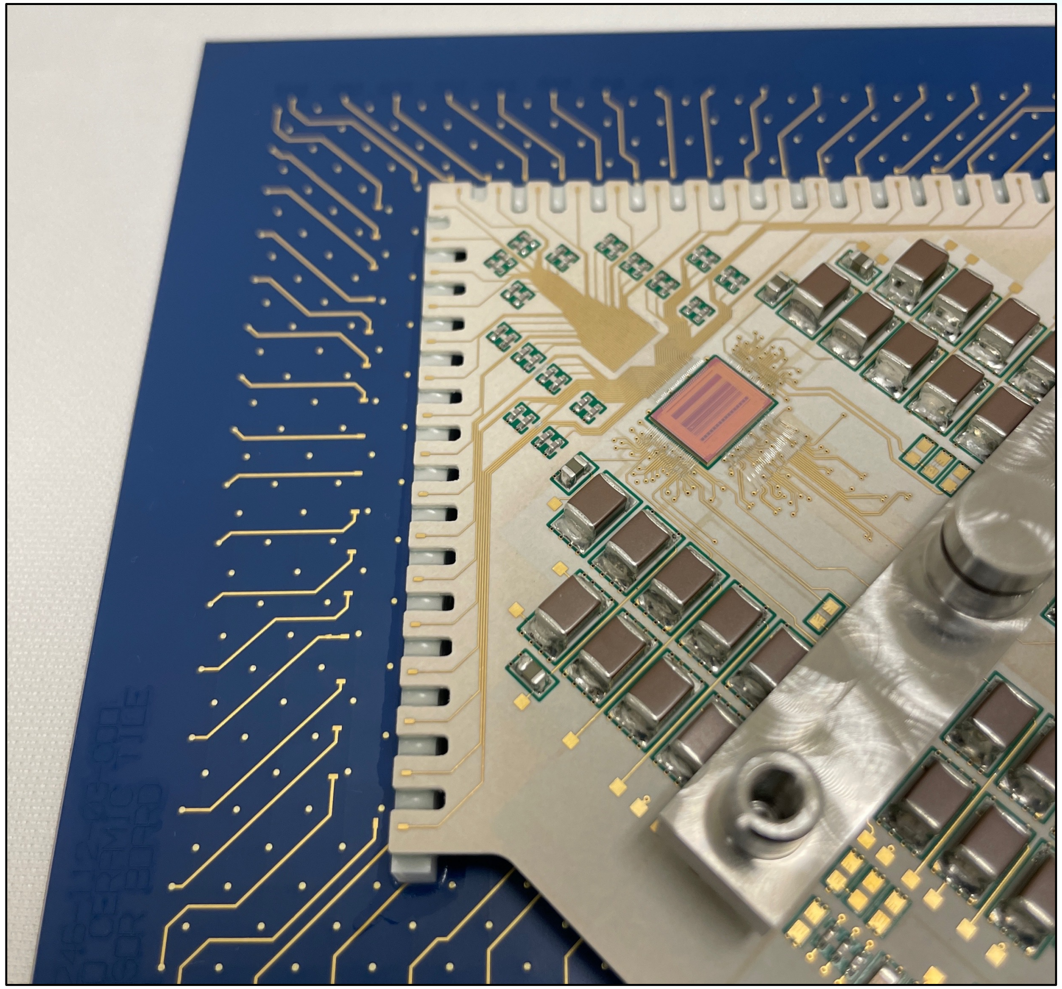


In addition to the standoffs, any components will be glued and wire-bonded instead of soldered (radiopurity)

Charge readout array would require approximately 10g of Masterbond

Assembled in a few cure cycles, using alignment jigs in a cleanroom





Key practical components

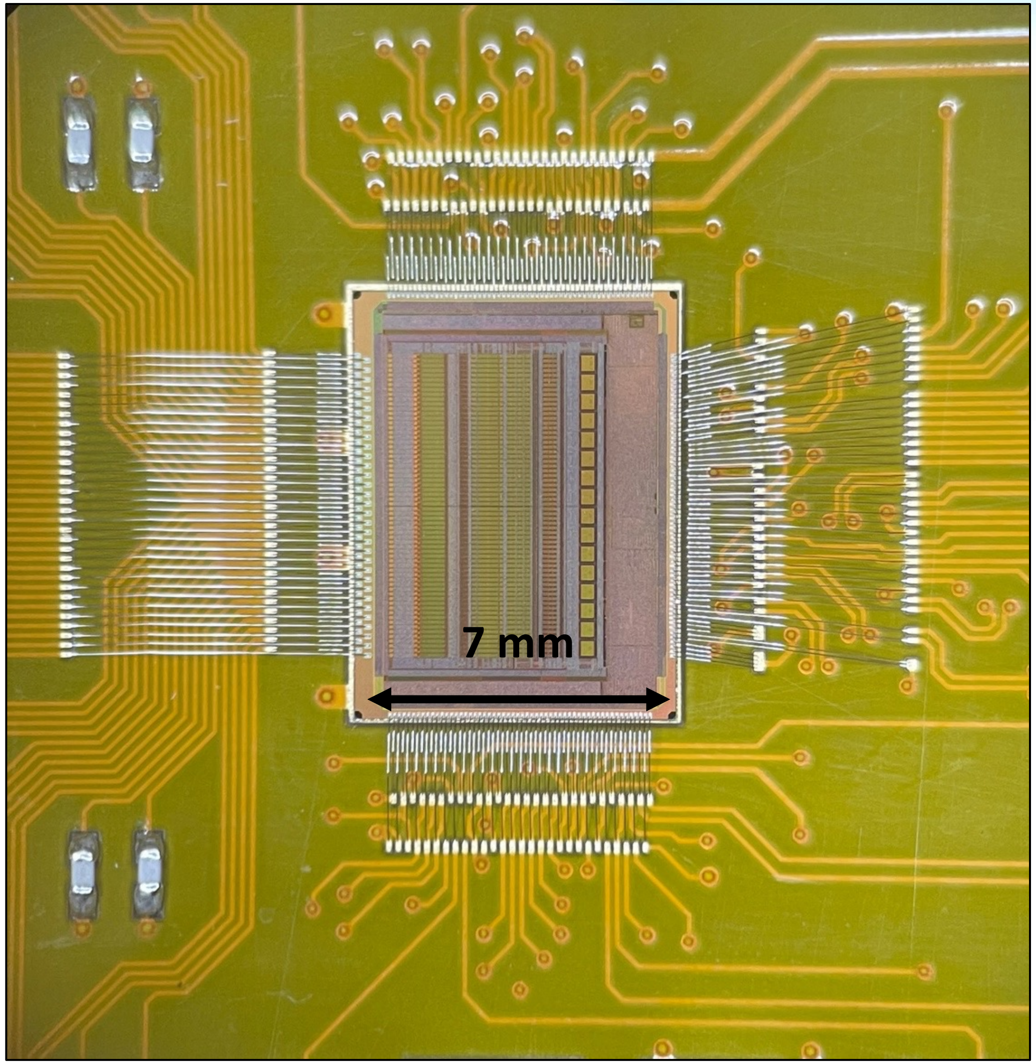
<u>Wire bonds</u>

- 100-150 bonds from ASIC-to-ASIC board
- 32 bonds from ASIC board to charge tile
- possibly 20 bonds from ASIC board to cable

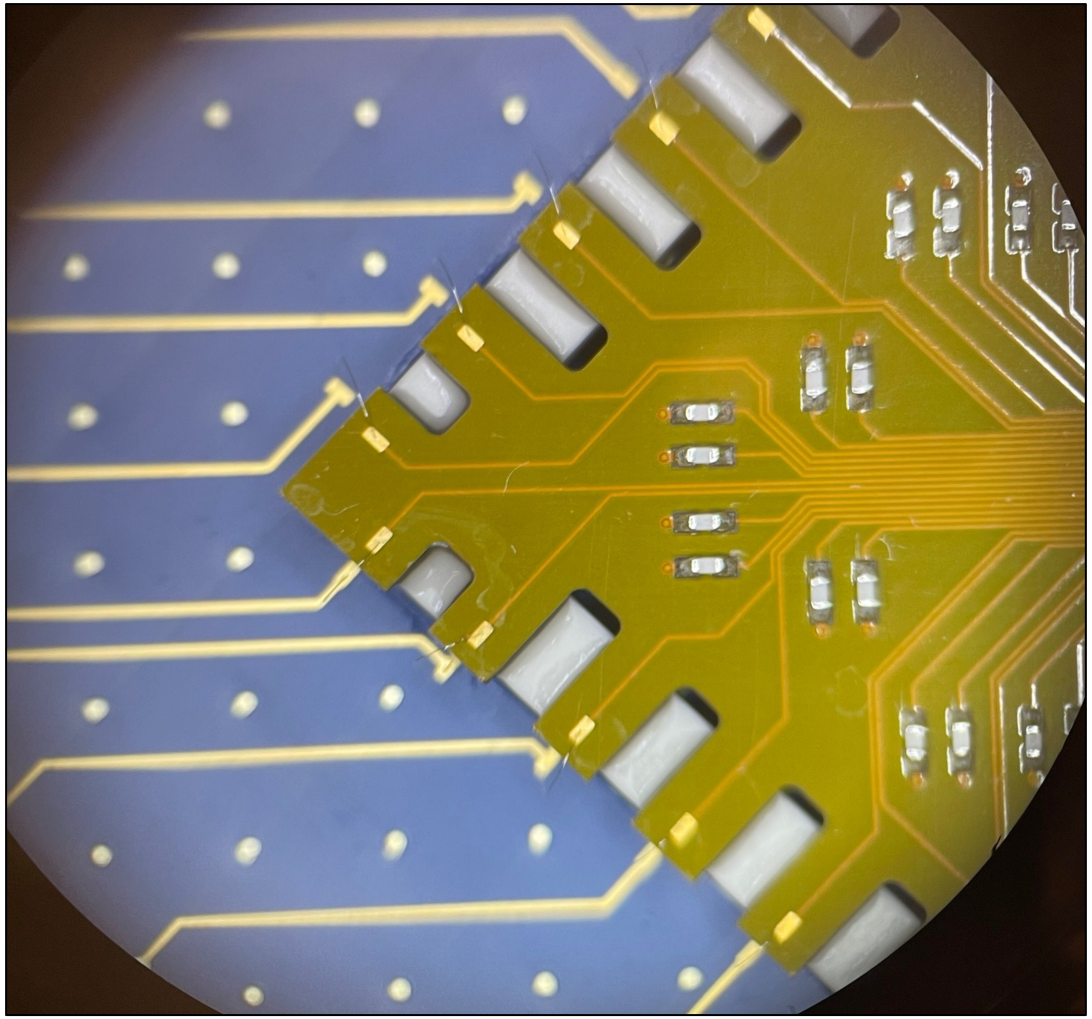
~20,000 wire-bonds on charge readout

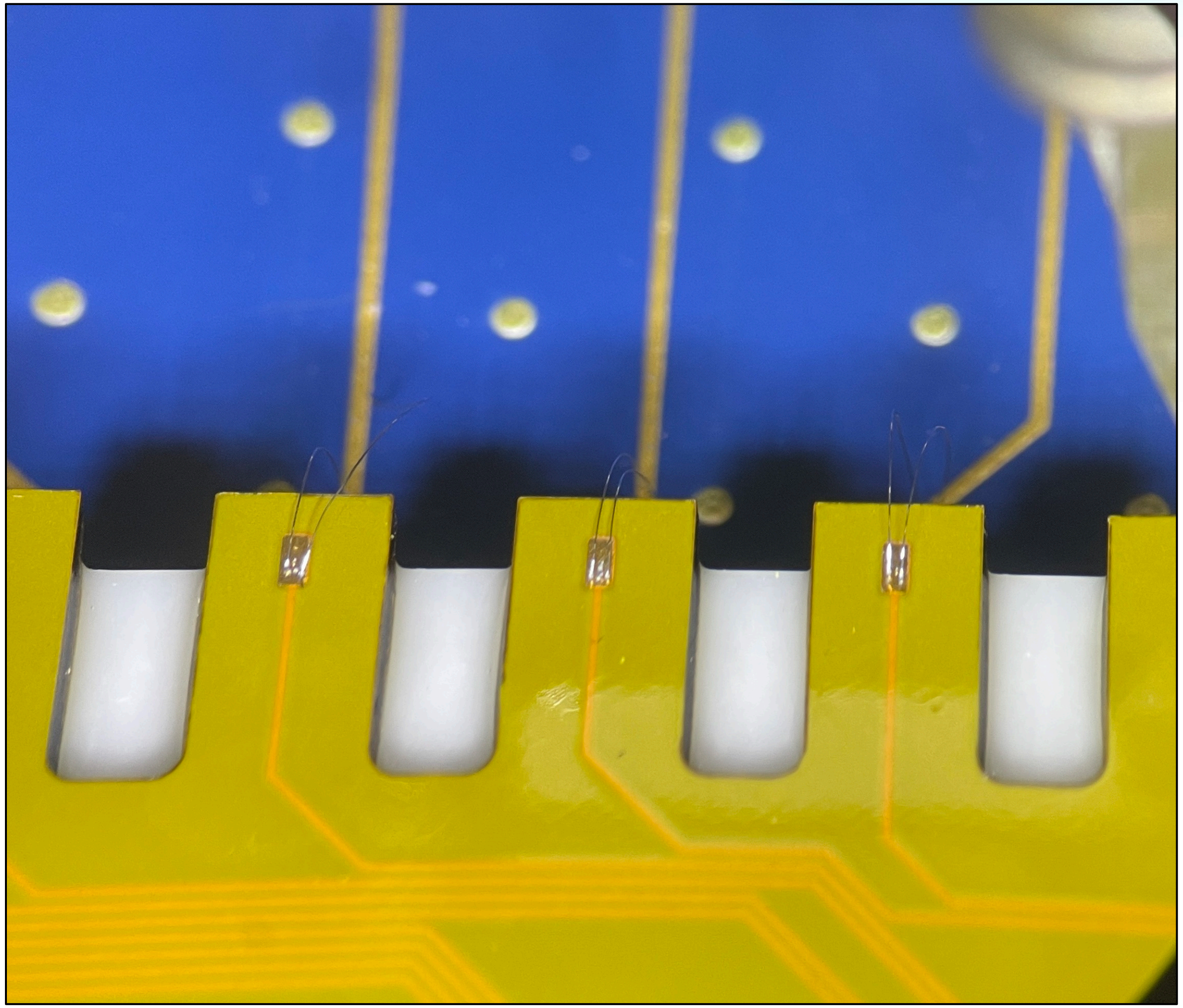
- 0.001” diameter aluminum
- Source of radiopure wire identified
- Failure rate is extremely small, but needs investigation
  - 30,000 in LCLS with no known failures

- Which forces in the liquid large enough to break or short bonds?

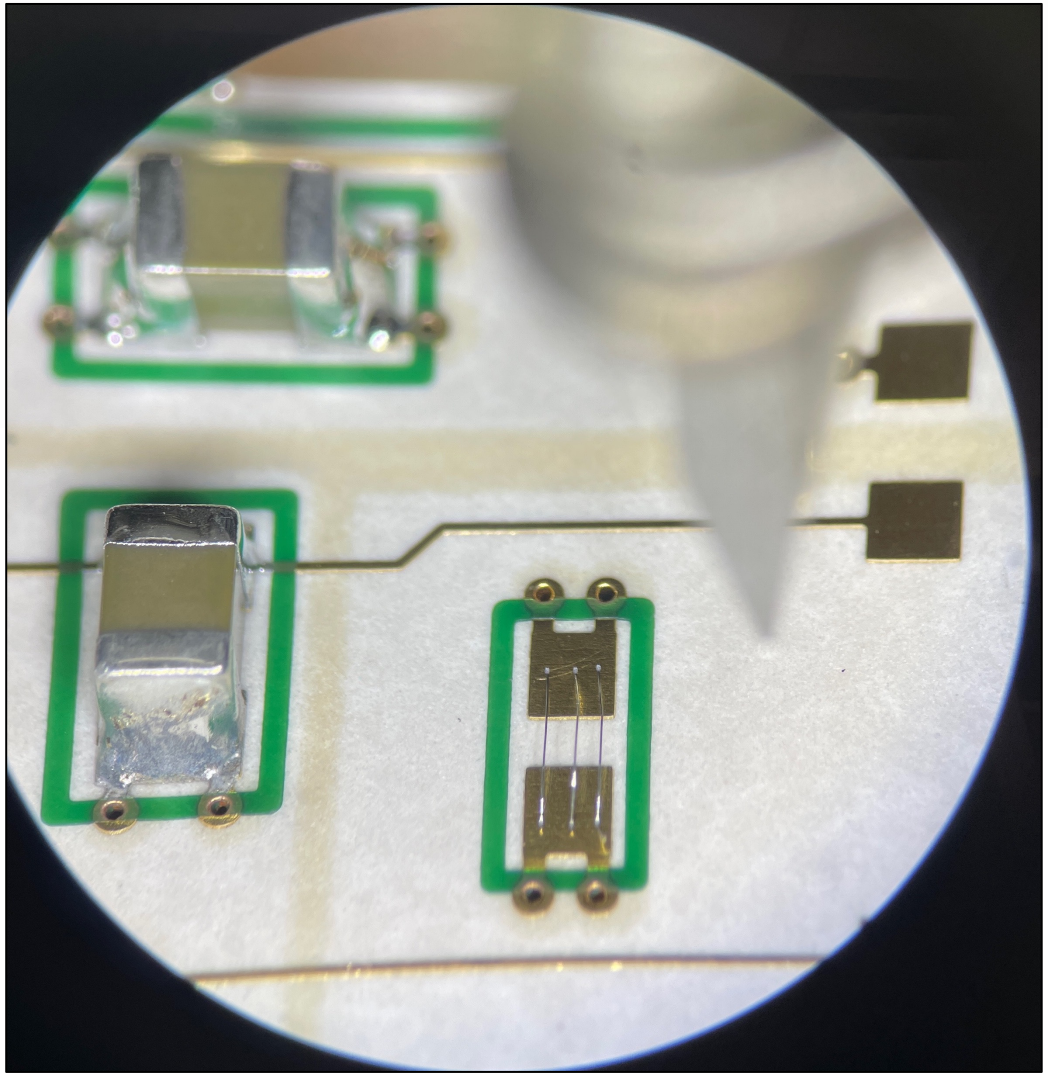


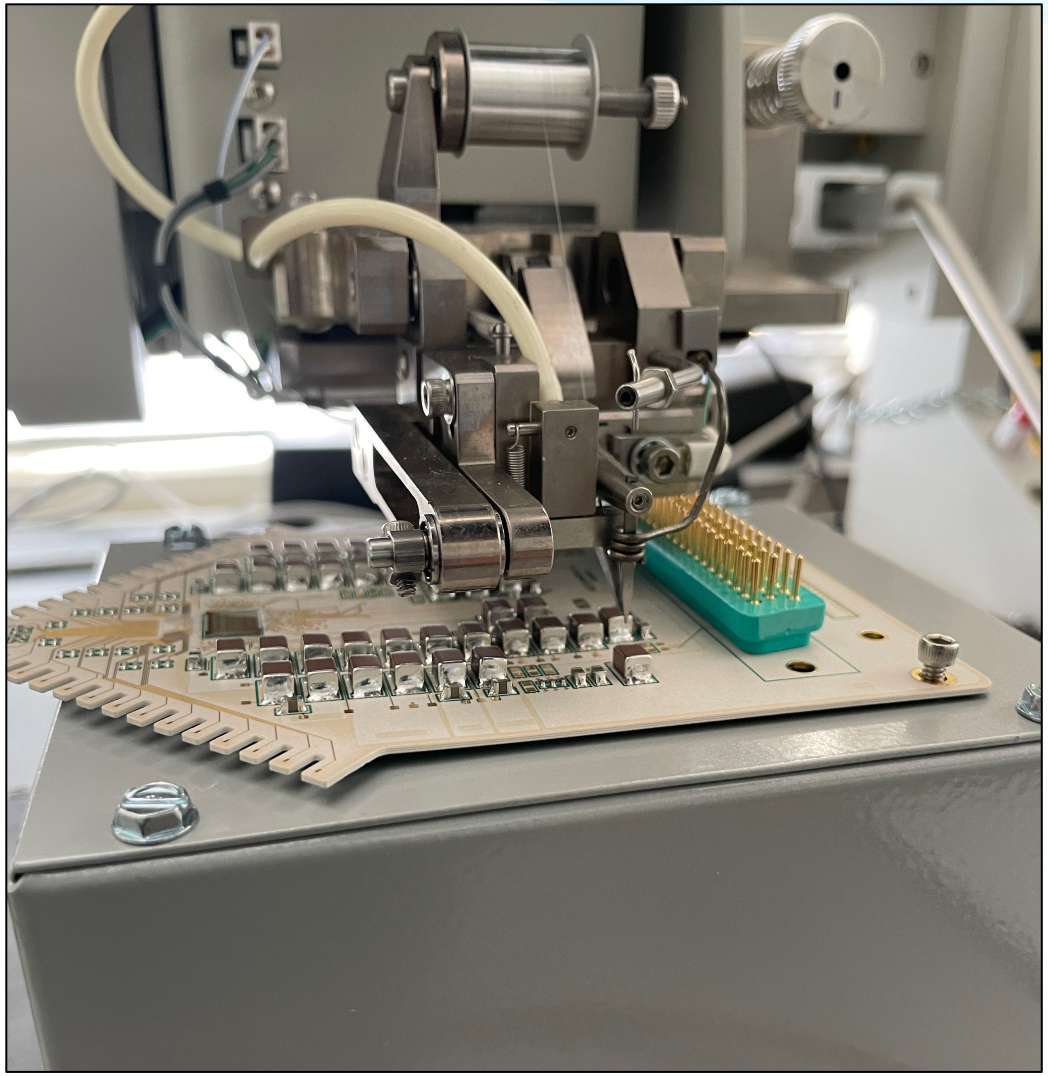
Key practical components





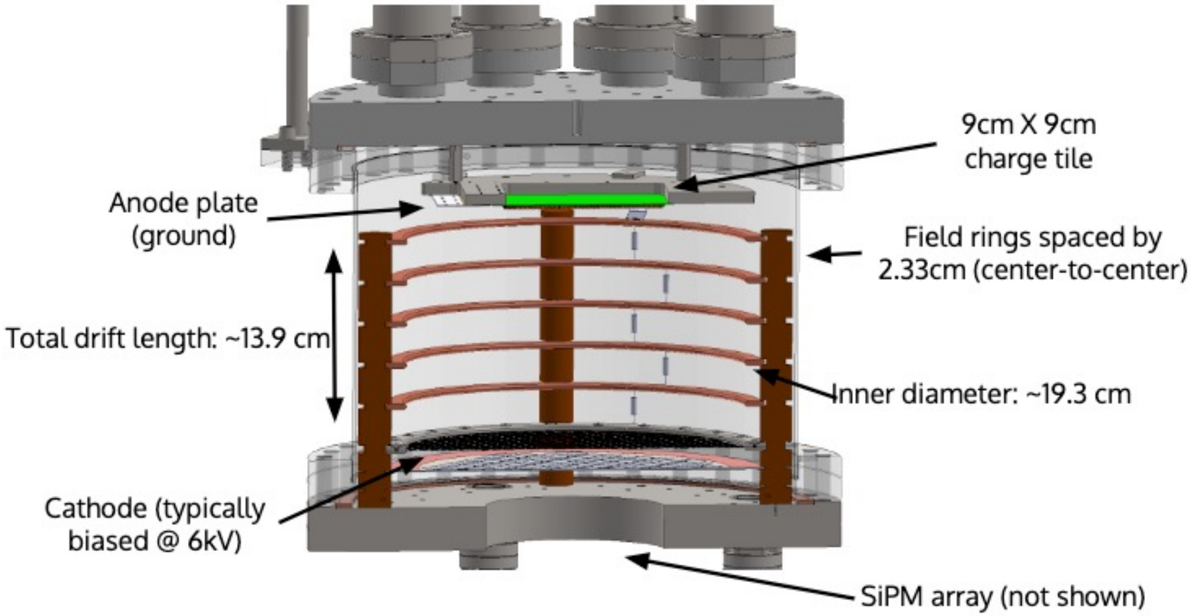
Key practical components

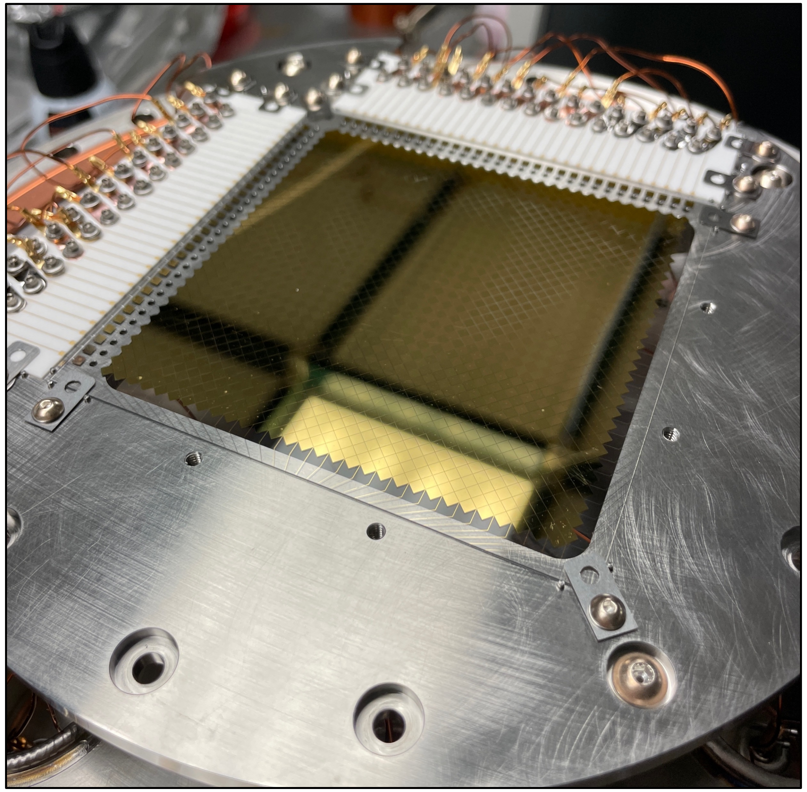




Prototype testing at Stanford

Use of a tile fabricated by IHEP/IME in 14 cm drift length to observe induction

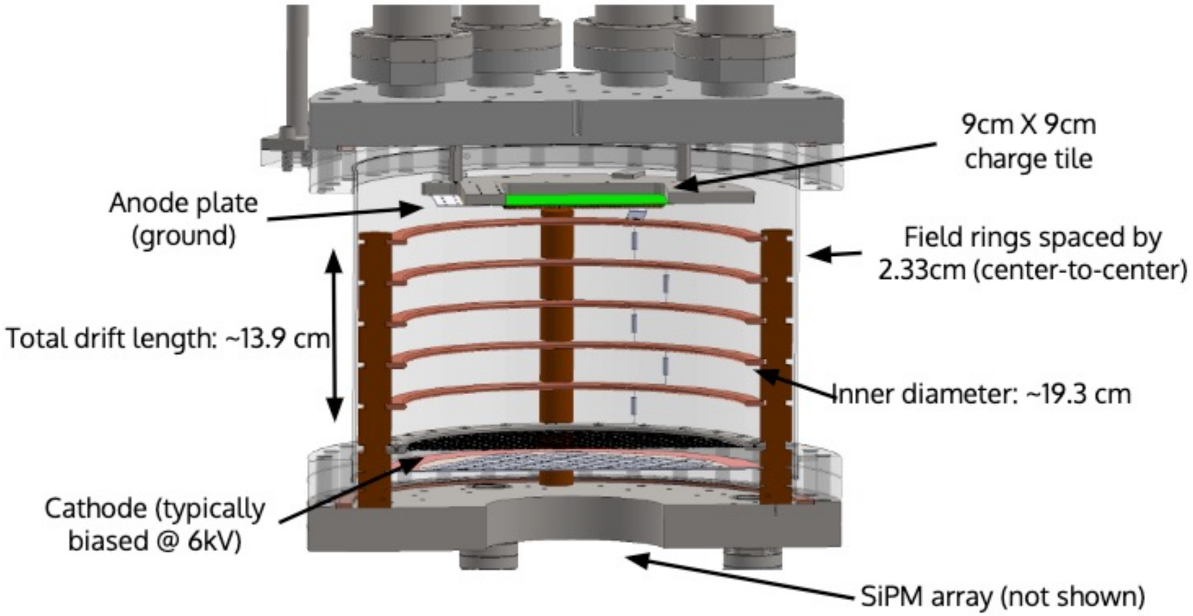




Stanford "Long" TPC

- Operating regularly ~30 kg LXe runs
- Can characterize detectors using internal/external radioactive sources

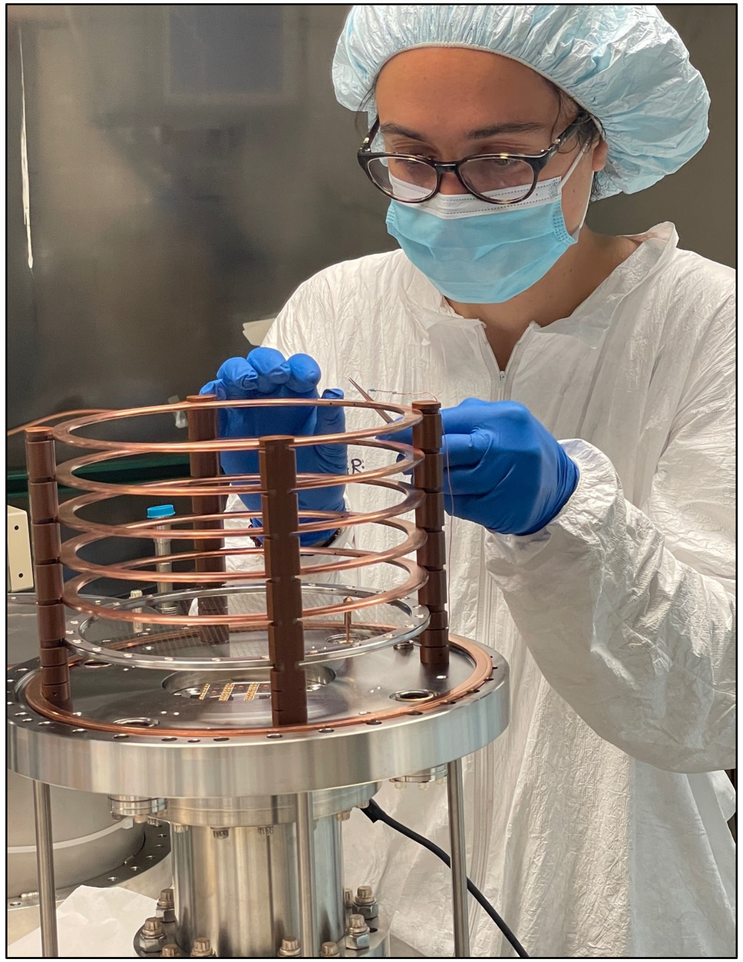
Prototype testing at Stanford



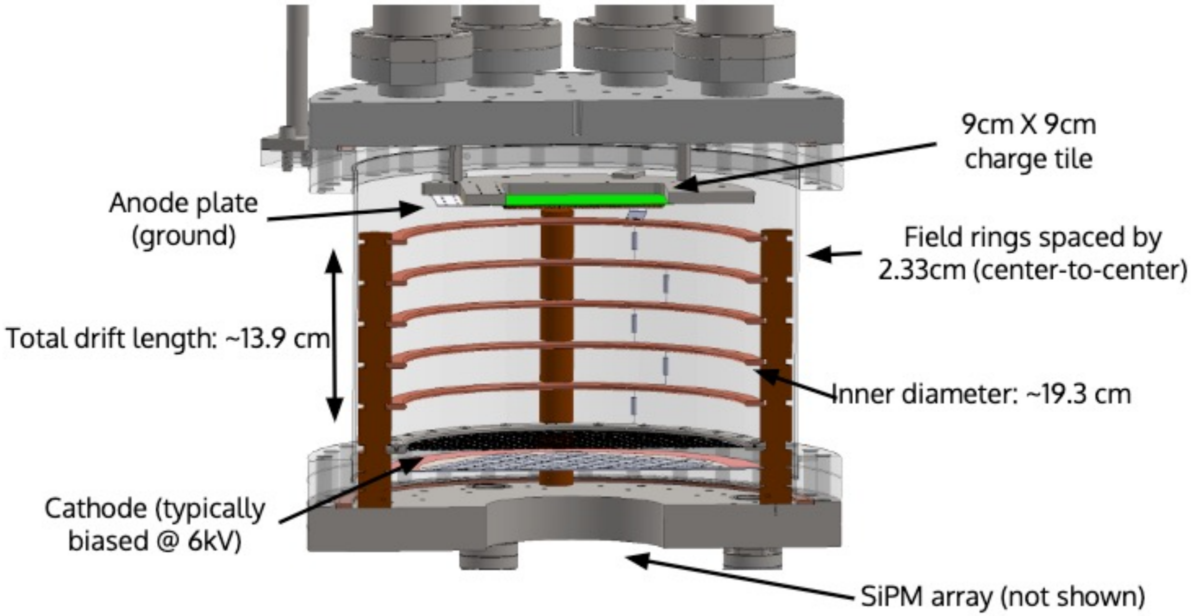
<u>Stanford "Long" TPC</u>

- Operating regularly ~30 kg LXe runs
- Can characterize detectors using internal/external radioactive sources

Marie Vidal assembling the TPC



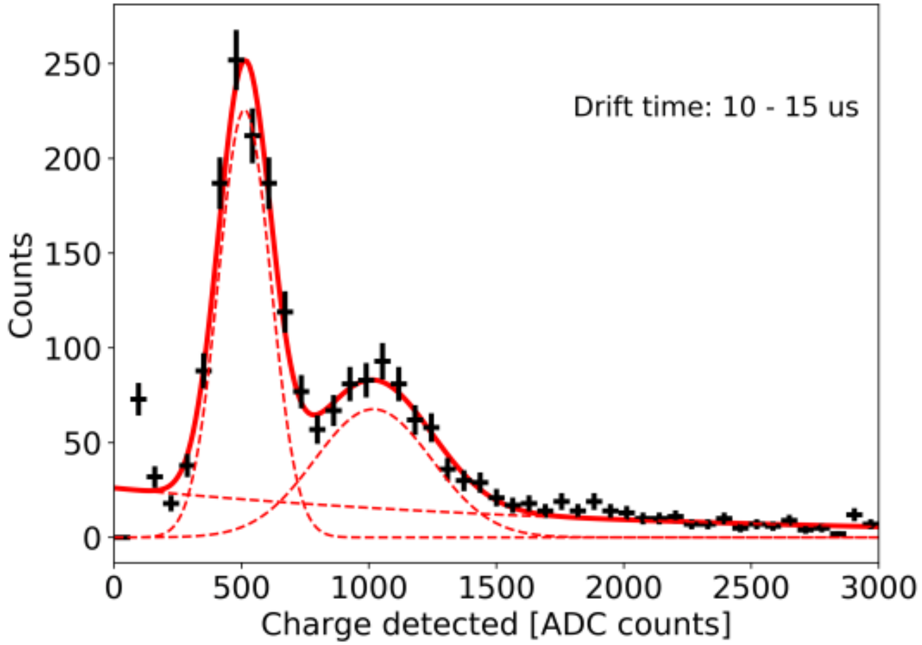
Prototype testing at Stanford



<u>Stanford "Long" TPC</u>

- Operating regularly ~30 kg LXe runs
- Can characterize detectors using internal/external radioactive sources

Measurement of injected ^{127}Xe source



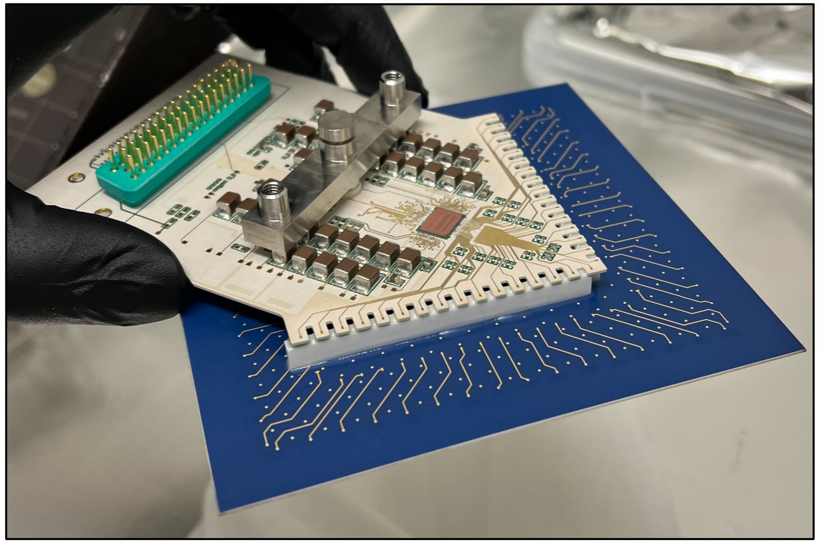
Lenardo, B. G., et al. "Development of a 127Xe Calibration Source for nEXO." Journal of Instrumentation 17, no. 07 (July 2022): P07028. https://doi.org/10.1088/1748-0221/17/07/P07028.

Summary

1. nEXO charge readout intimately relates to the three main measurables of nEXO: energy, multi-site/single-site, standoff

2. nEXO uses a modular array of charge collection tiles that can support electronics directly attached

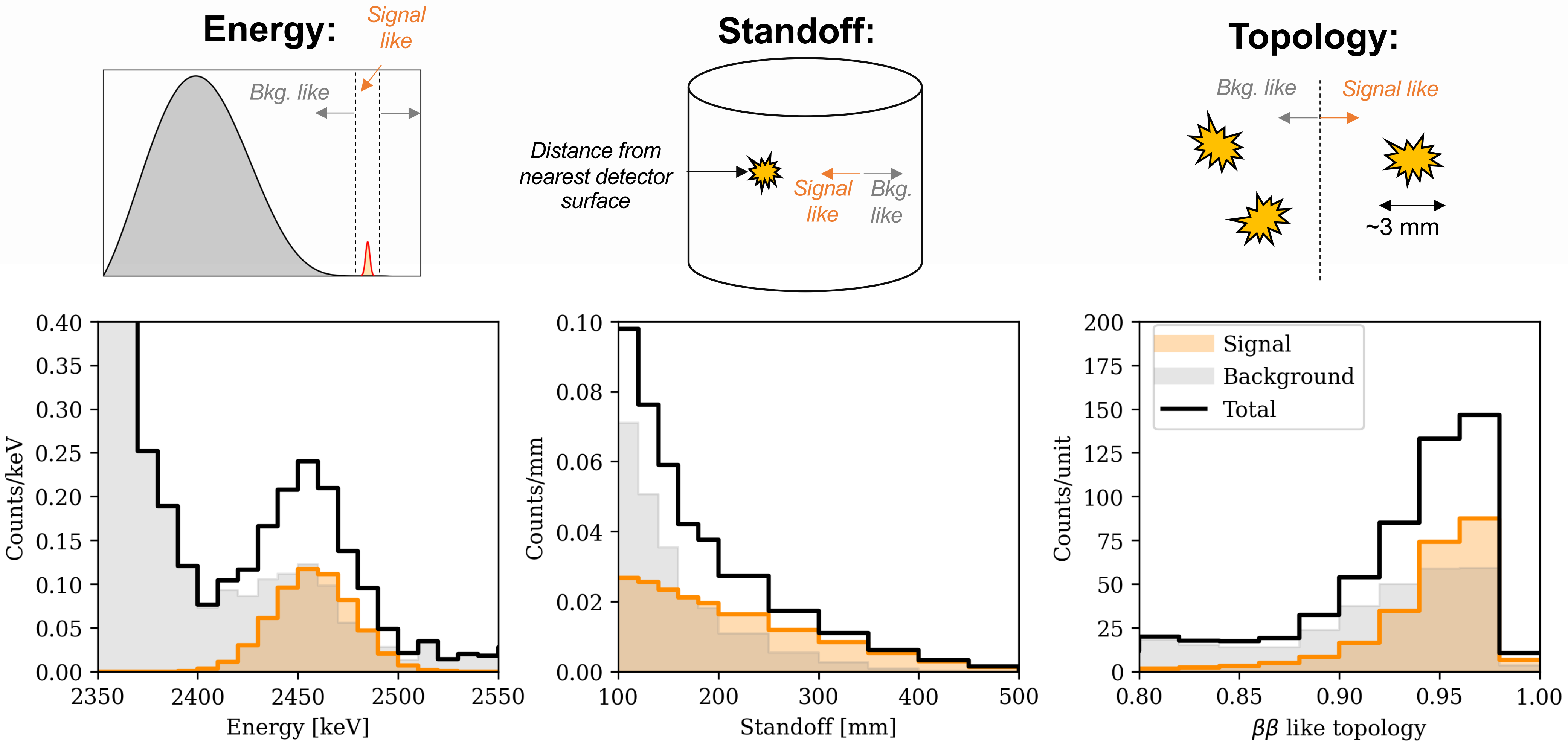
3. Amplifying and digitizing in the liquid



Prototype CRYO ASIC + Tile modules soon to measure sources in LXe

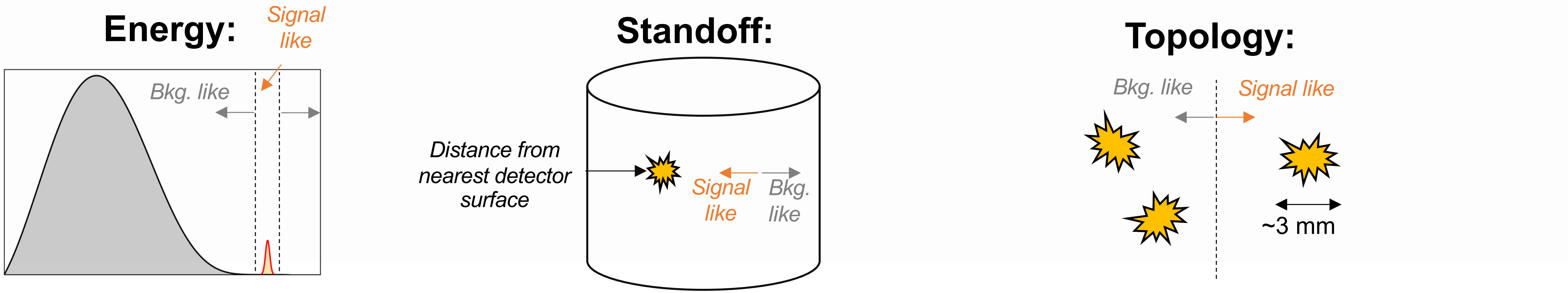
Backup

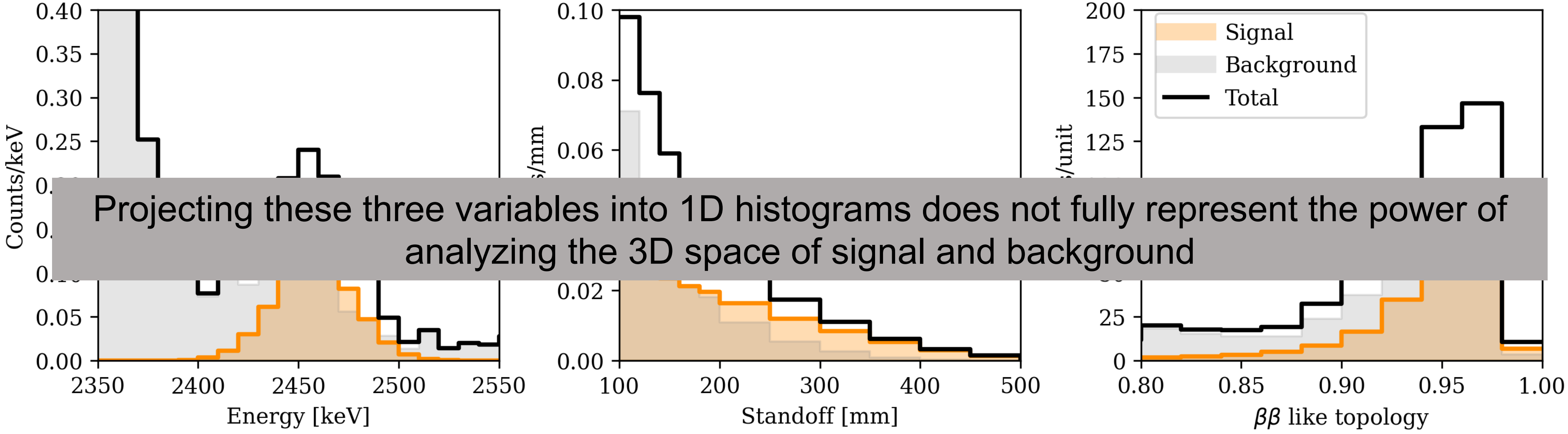
An analysis using all observables cohesively



(shows an example where the $0\nu\beta\beta$ half-life is 7.4 x 10^{27} yr and we observe until 3-sigma discovery is made)

An analysis using all observables cohesively



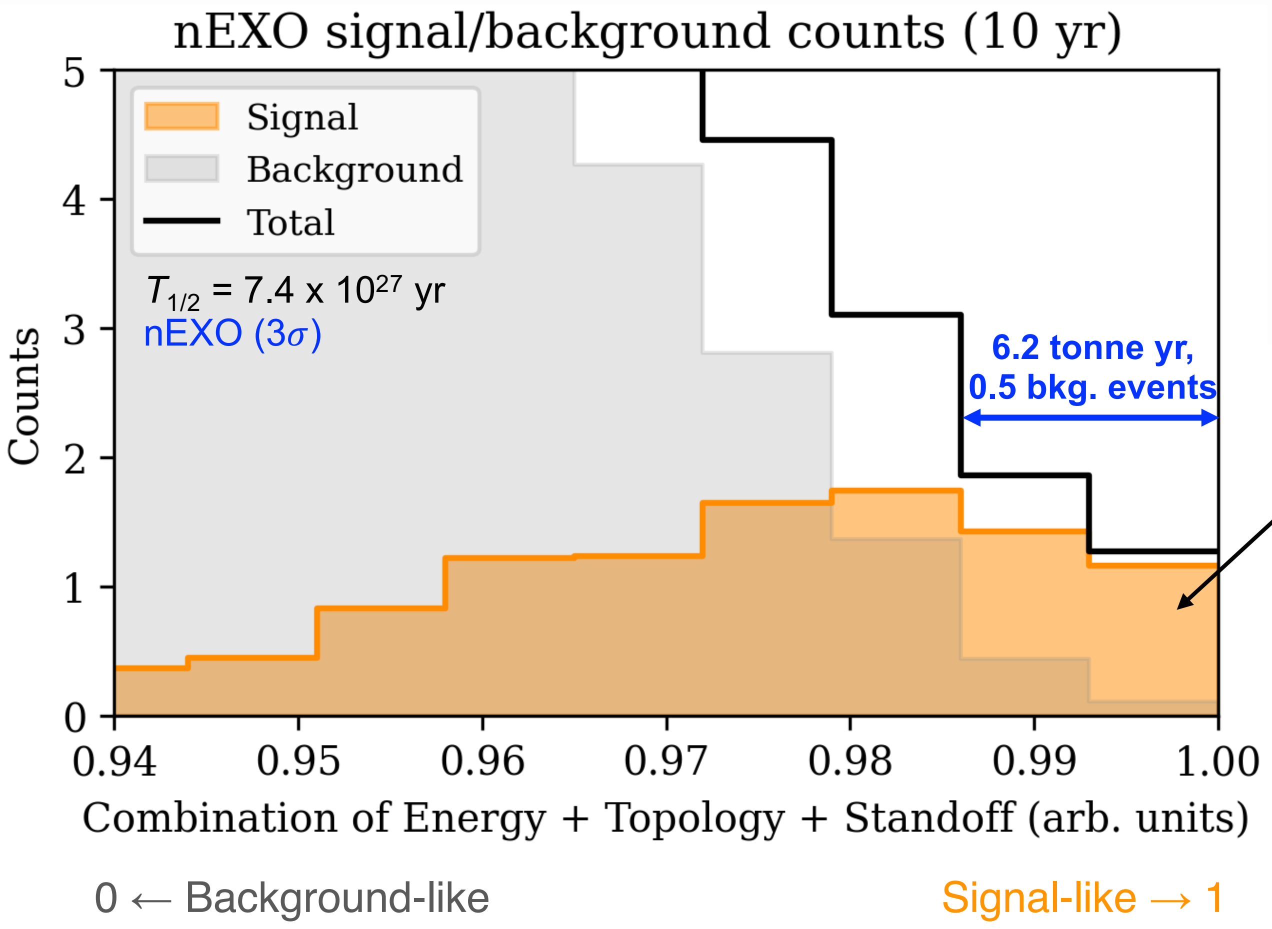


Projecting these three variables into 1D histograms does not fully represent the power of analyzing the 3D space of signal and background

(shows an example where the $0\nu\beta\beta$ half-life is 7.4 x 10^{27} yr and we observe until 3-sigma discovery is made)

An analysis using all observables cohesively

nEXO



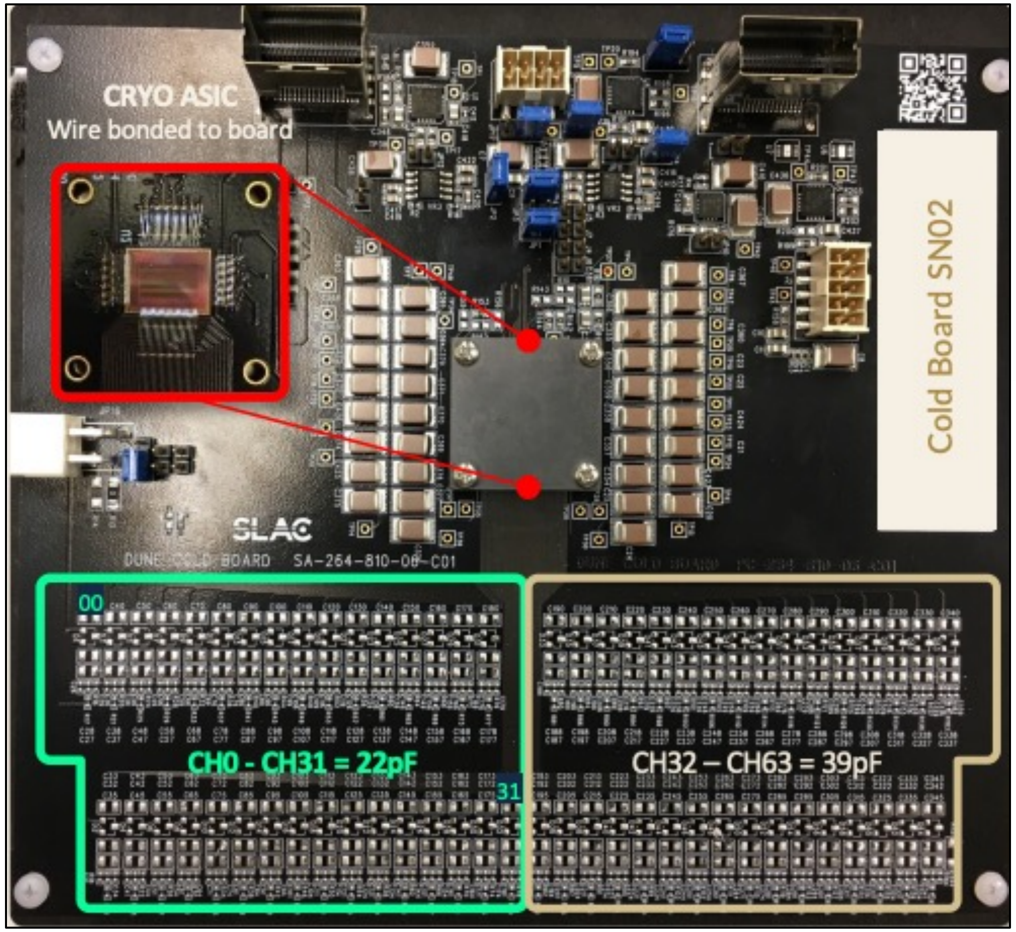
In the 3D histogram of observables, there is a region highly pure in signal events, ordered on this histogram sequentially

In summary:

- **Energy resolution is important but is not the only quantity that enables discovery** (in nEXO <1% when light and charge are used in combination)
  - $2\nu\beta\beta$ overlaps with $0\nu\beta\beta$ in energy space with a negligable background of 0.8% of all SS events / (2000 kg x FWHM)
- **nEXO is not a counting experiment, uses multiple observables**

UCSD tests with lumped capacitors

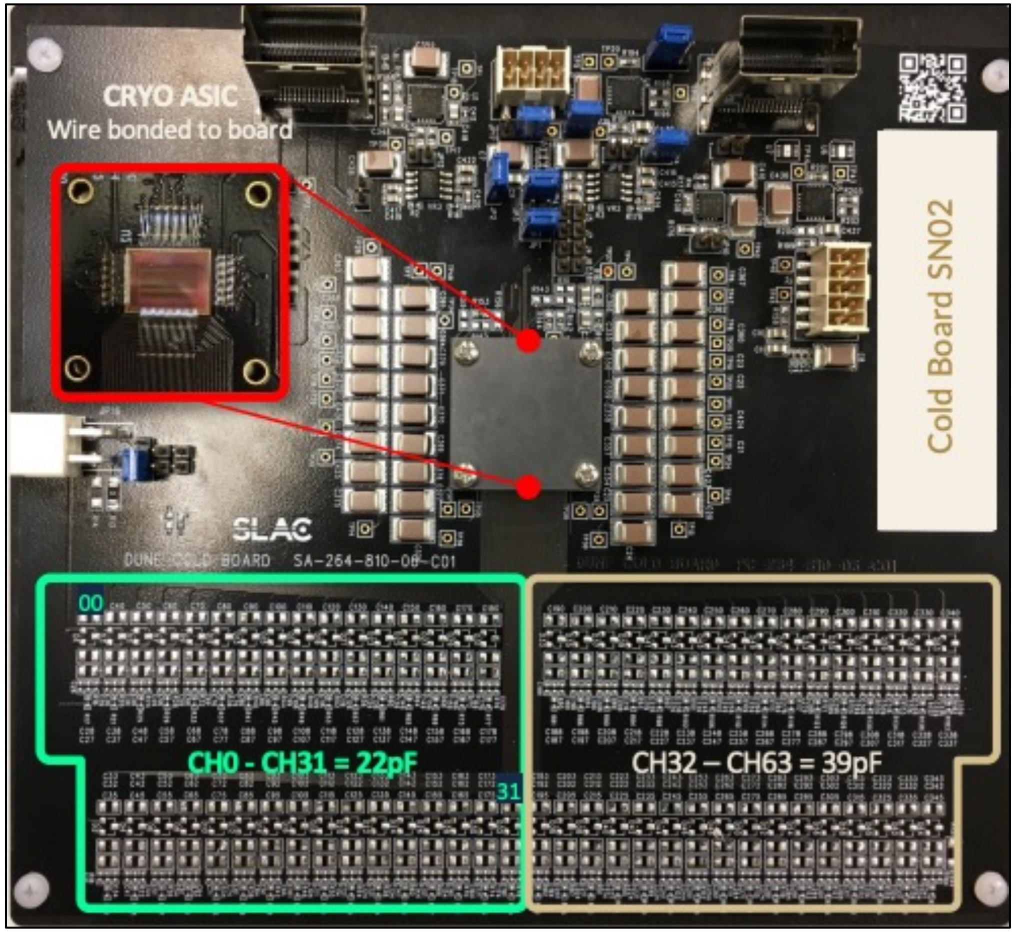
UCSD team includes Liang Yang, Zepeng Li, and students



Environmental chamber cooled with LN2

UCSD tests with lumped capacitors

UCSD team includes Liang Yang, Zepeng Li, and students

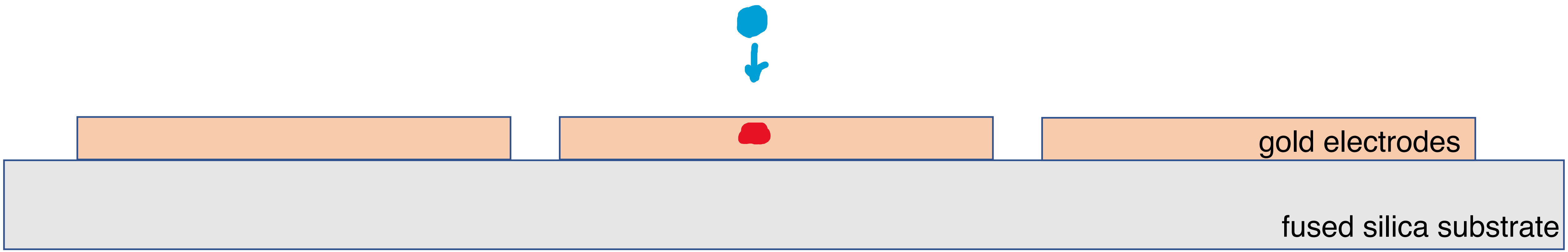


Detection of charges, induction, and weight potential

As charges get close to electrodes, they induce an opposite charge (pulling that charge from the input of an amplifier, for example)

the induced charge is a function of position, and must be proportional to the quantity of charge drifting

$$Q_{ind} = Q_0 \psi(\mathbf{x})$$



Detection of charges, induction, and weight potential

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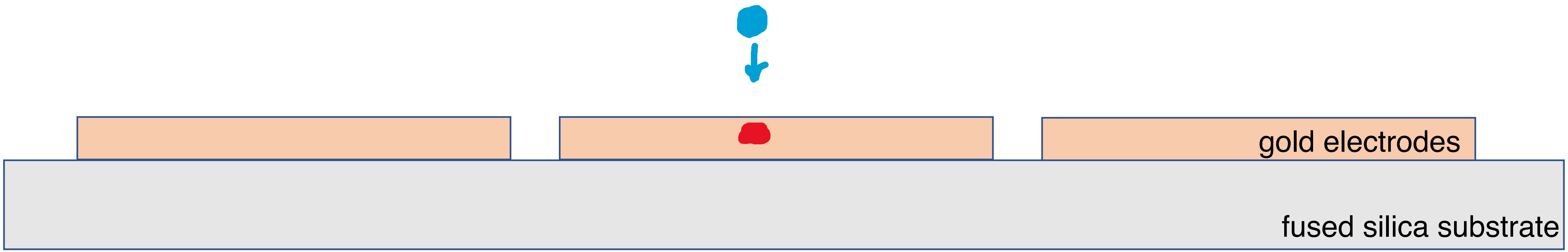
the induced charge is a function of position, and must be proportional to the quantity of charge drifting

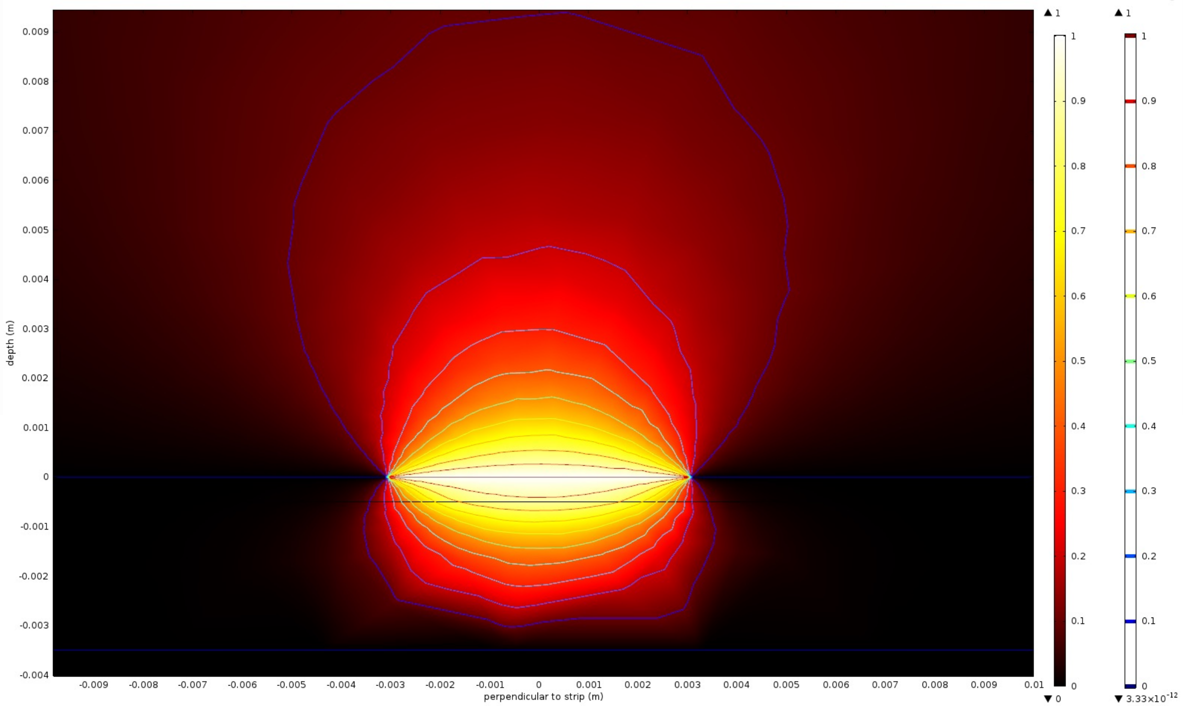
$$Q_{ind} = Q_0 \psi(\mathbf{x})$$

the magic of the **"Weight Potential"** is that it is also equal to the electric scalar potential with that electrode set to 1V and everything else set to 0V

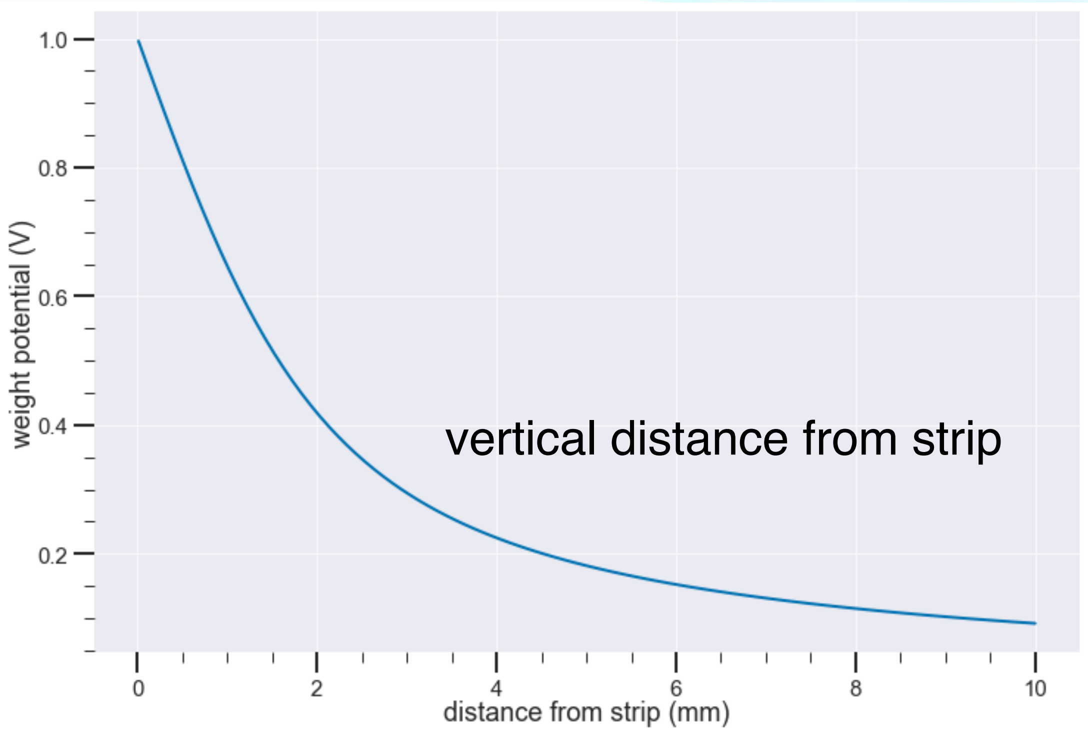


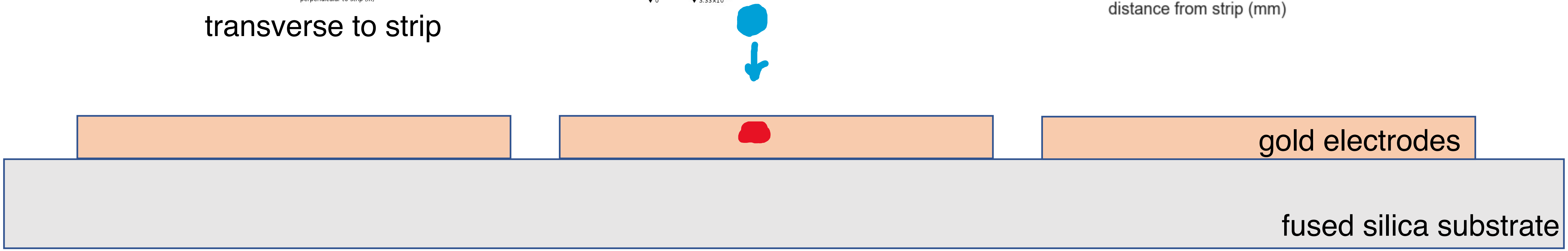
Detection of charges, induction, and weight potential

nEXO



transverse to strip





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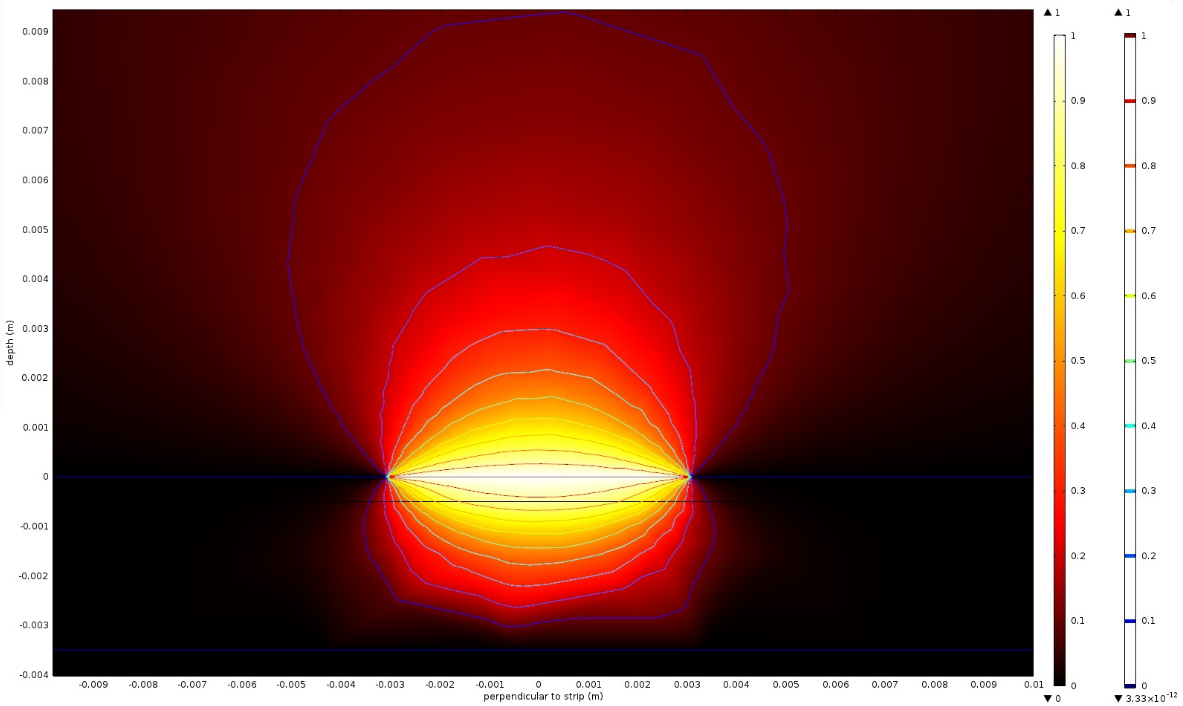
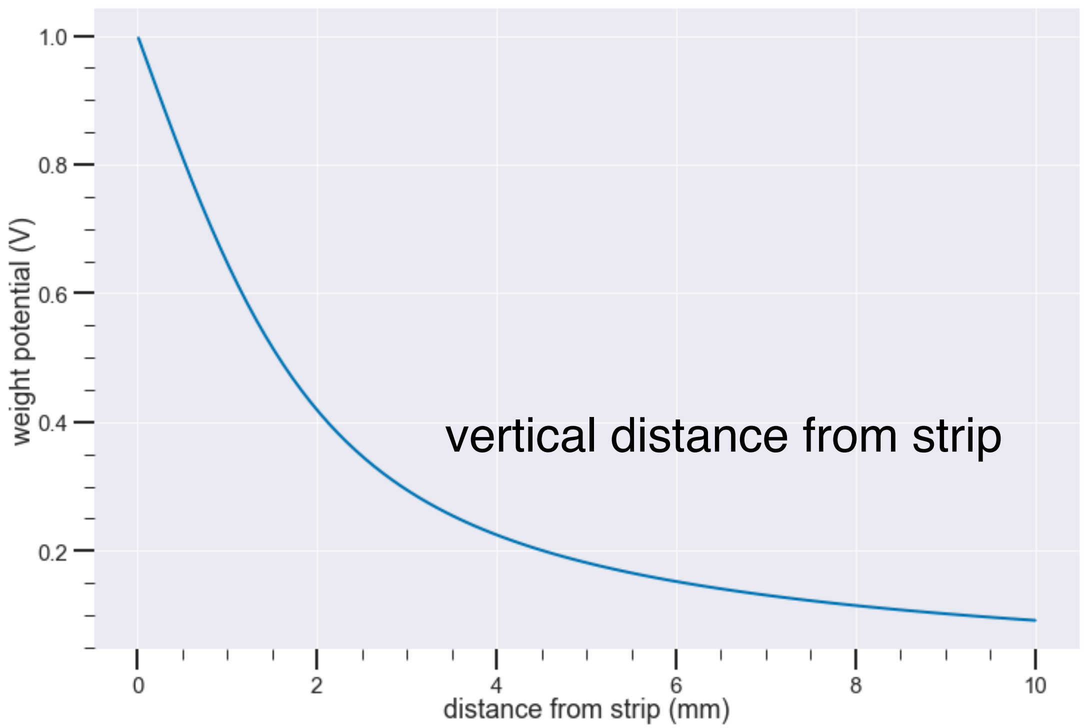


transverse to strip



The length-scale (and thus time scale in a TPC) for a rising induced electrical signal is set by the length of the strip

We build test TPCs at Stanford that have drift lengths on order >10 cm

Prototype ASIC Board

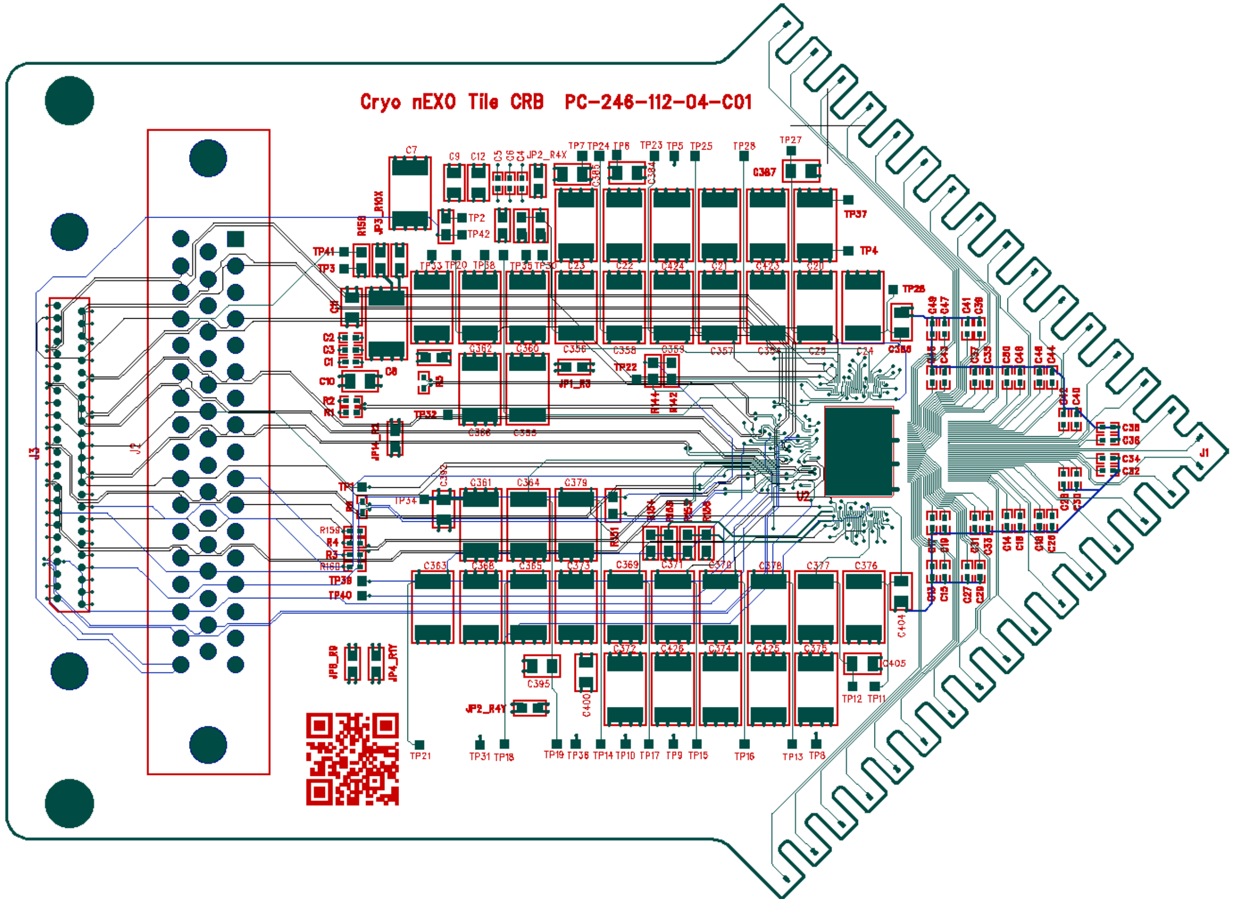
Functions:

- Houses the ASIC and power planes for ASIC
(200 pins, 500 MHz data lines, tens of power planes)

- Lifts those gnd/power planes away from the strips
(reduce detector capacitance, modularity)

- Supports components for power decoupling

- Input/output connectors



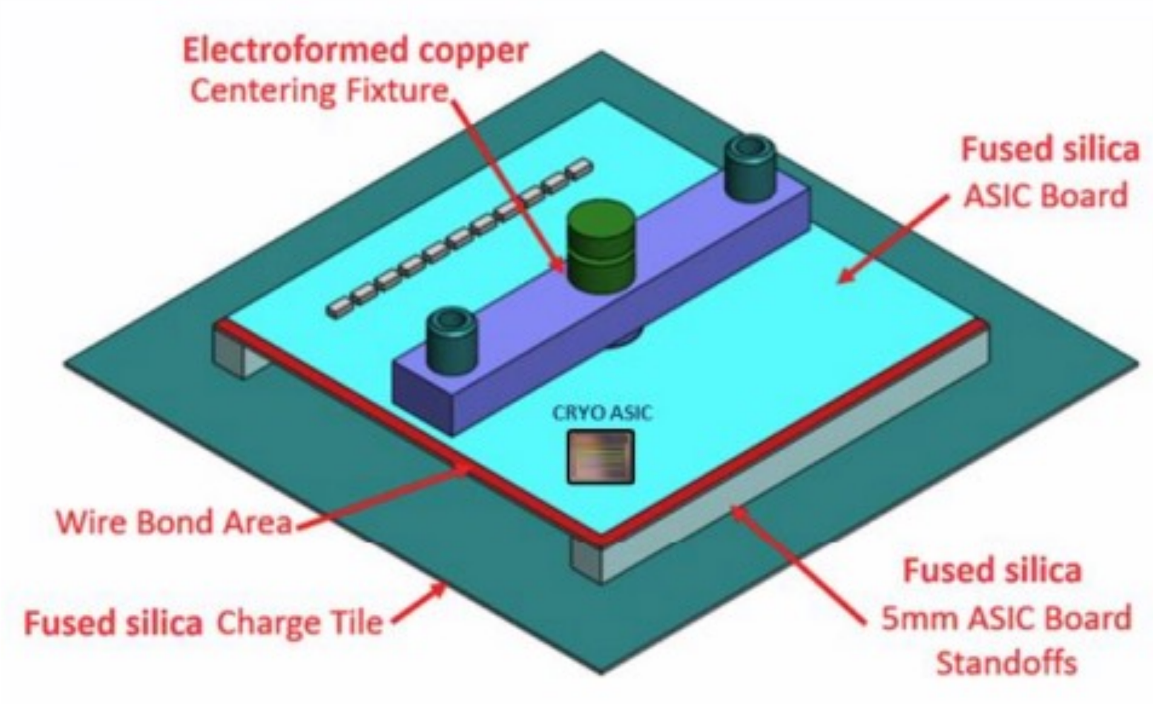
Resulting requirements:

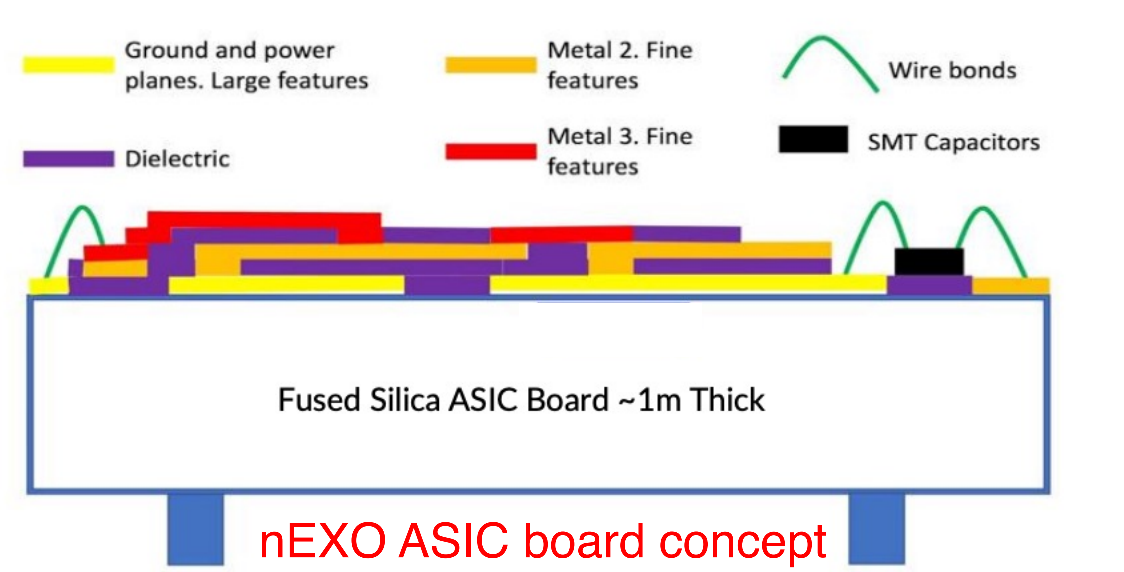
- Many layers

- Multiple sources of electronegative impurities

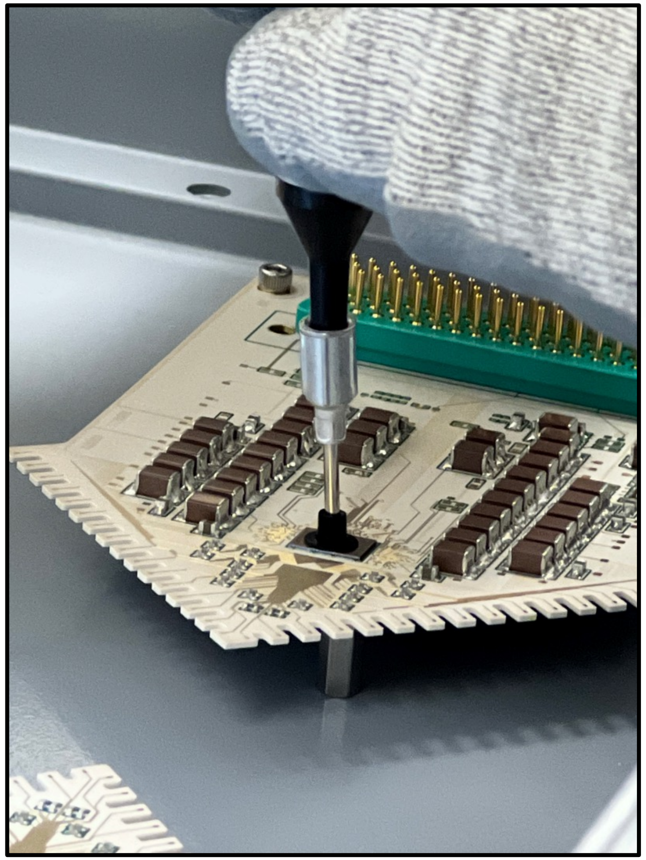
nEXO ASIC board develops in parallel with prototype ASIC board and tile testing

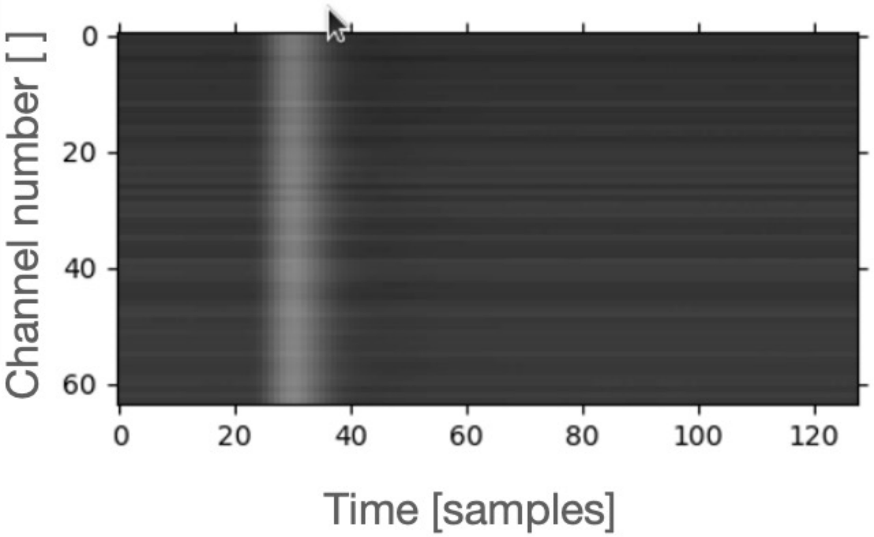
Radiopurity constraints mean that the nEXO ASIC board is a fused silica, photolithographic/CVD fabricated PCB from the SLAC team, Chris Kenney's group

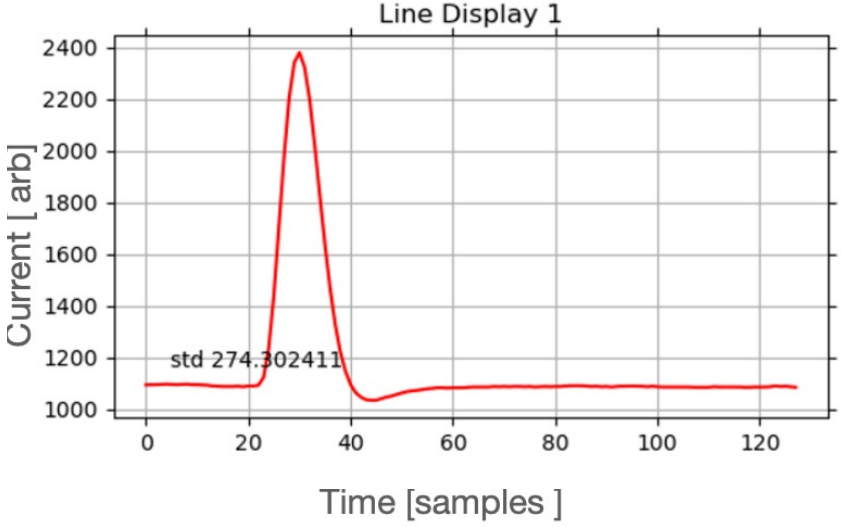




Bench-top testing







Firmware and software with GUI user interface is mature and operating at multiple test institutions

Two boards tested on the bench, working as expected